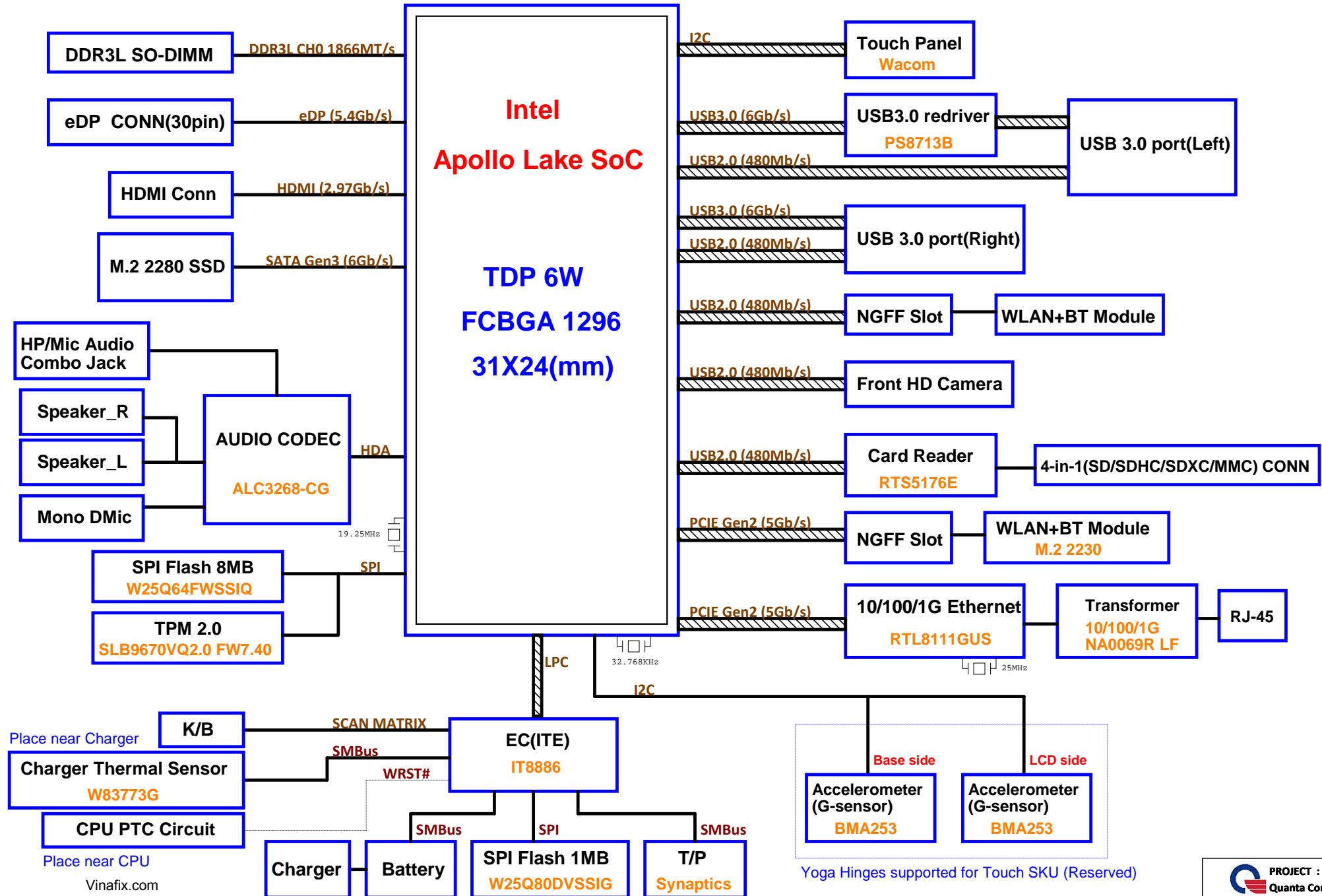
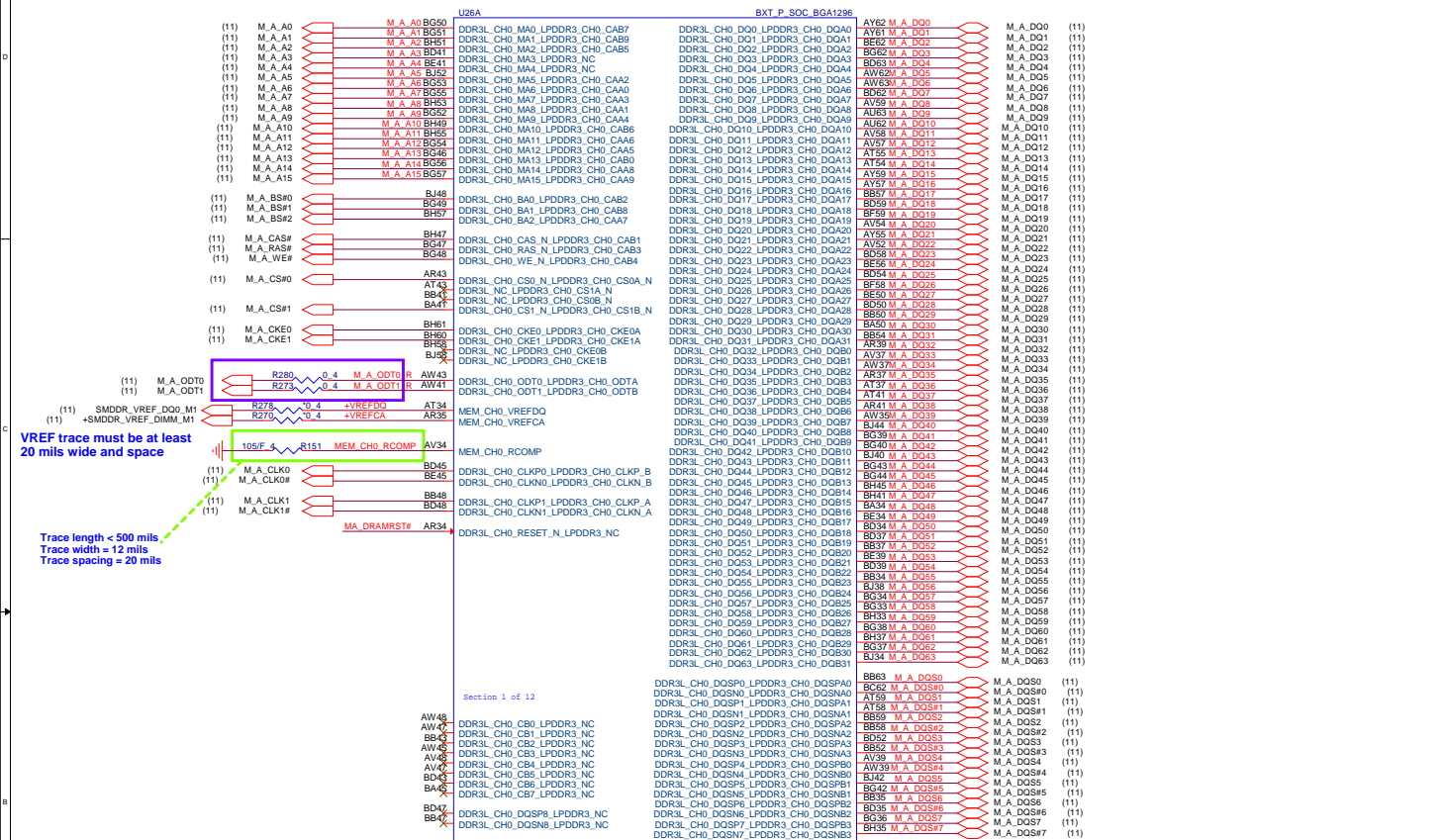
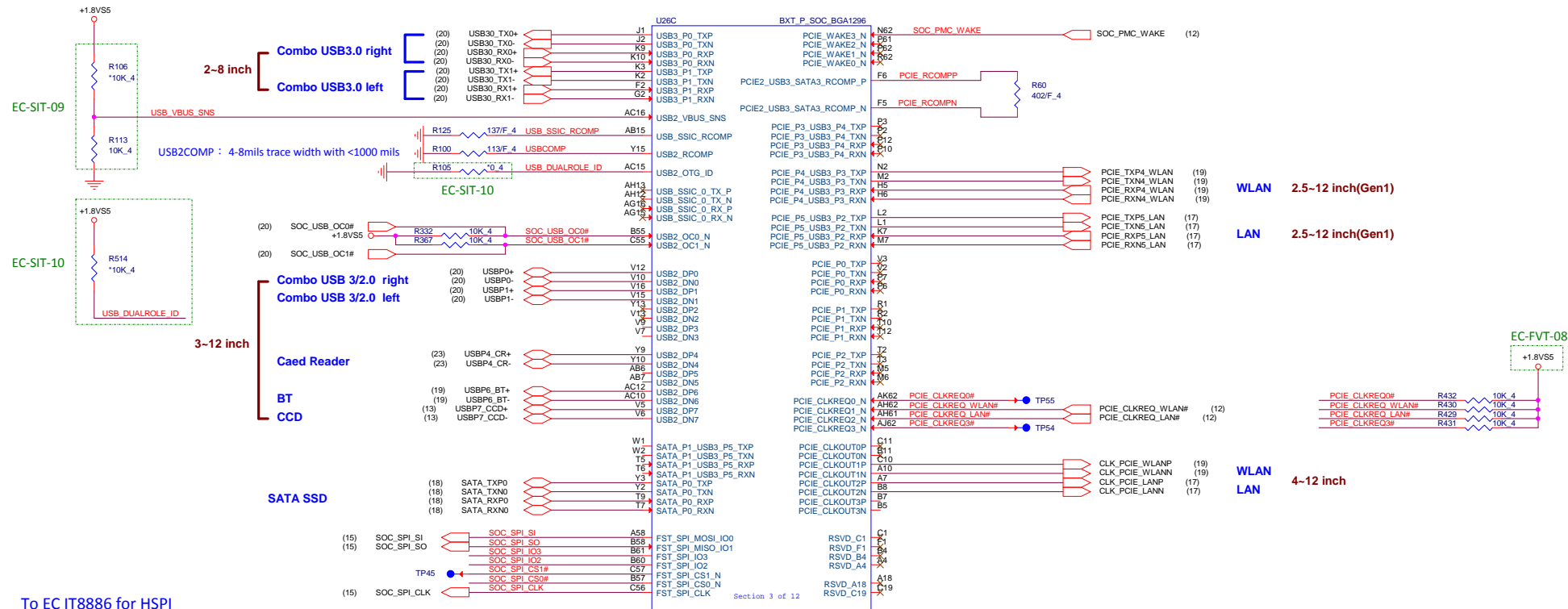


Newton II Intel APL Platform UMA Block Diagram (Windows)

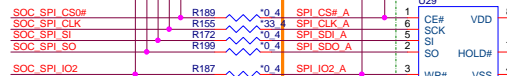
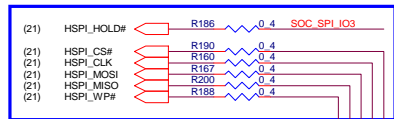


(7,11,28,35) +1.35VSUS

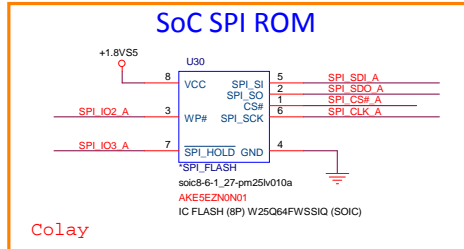
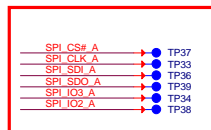




To EC IT8886 for HSPI



Placment Top side



SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	8MB	AKE5EZN0N01	W25Q64FWSSIQ



PROJECT : LI8G
Quanta Computer Inc.

Apollolake (DISPLAY,eDP)

(3,5,6,7,9,10,12,14,15,21,29,31,33,35)
(6,12,13,14,18,21,33)
(6,11,12,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,32,33)

+1.8VSS
+1.8V
+3.3V

04

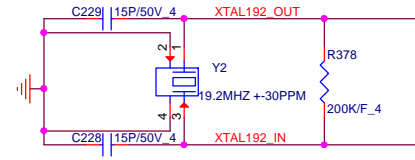
Max 7.5 inch HDMI

(14) IN_D2
(14) IN_D2#
(14) IN_D1
(14) IN_D1#
(14) IN_D0
(14) IN_D0#
(14) IN_CLK
(14) IN_CLK#

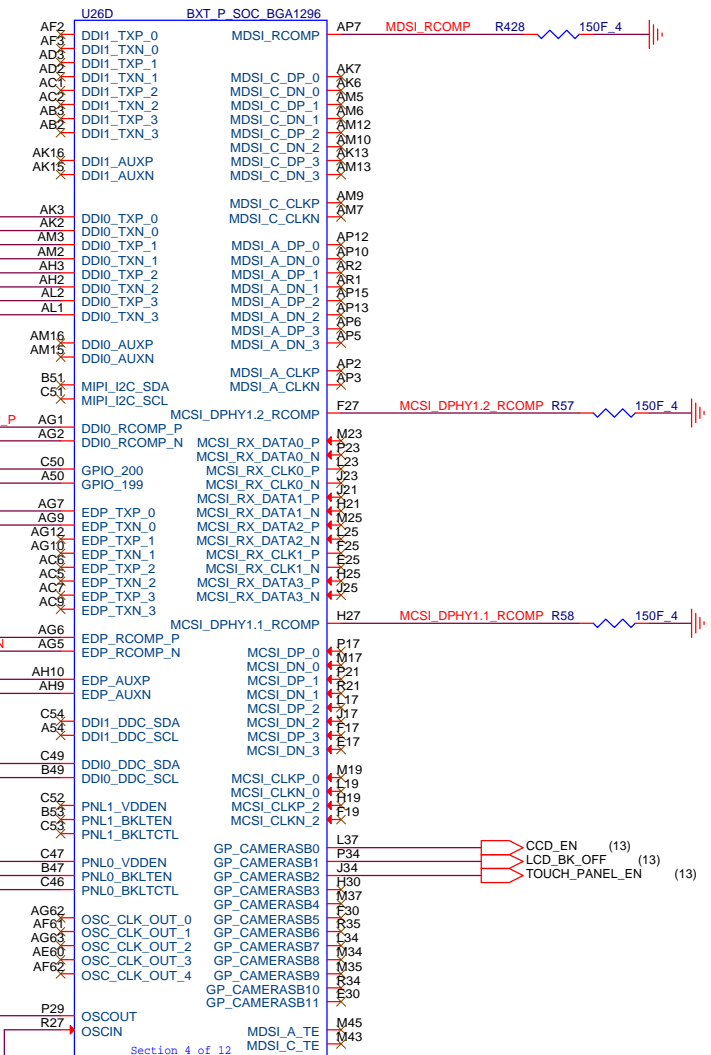
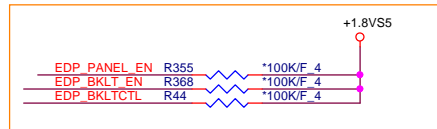
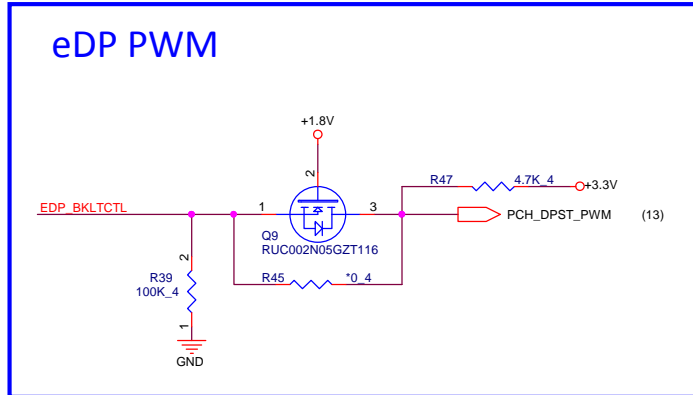
DDIO_HPD
DDI1_HPD

eDP Panel

<10000 mil

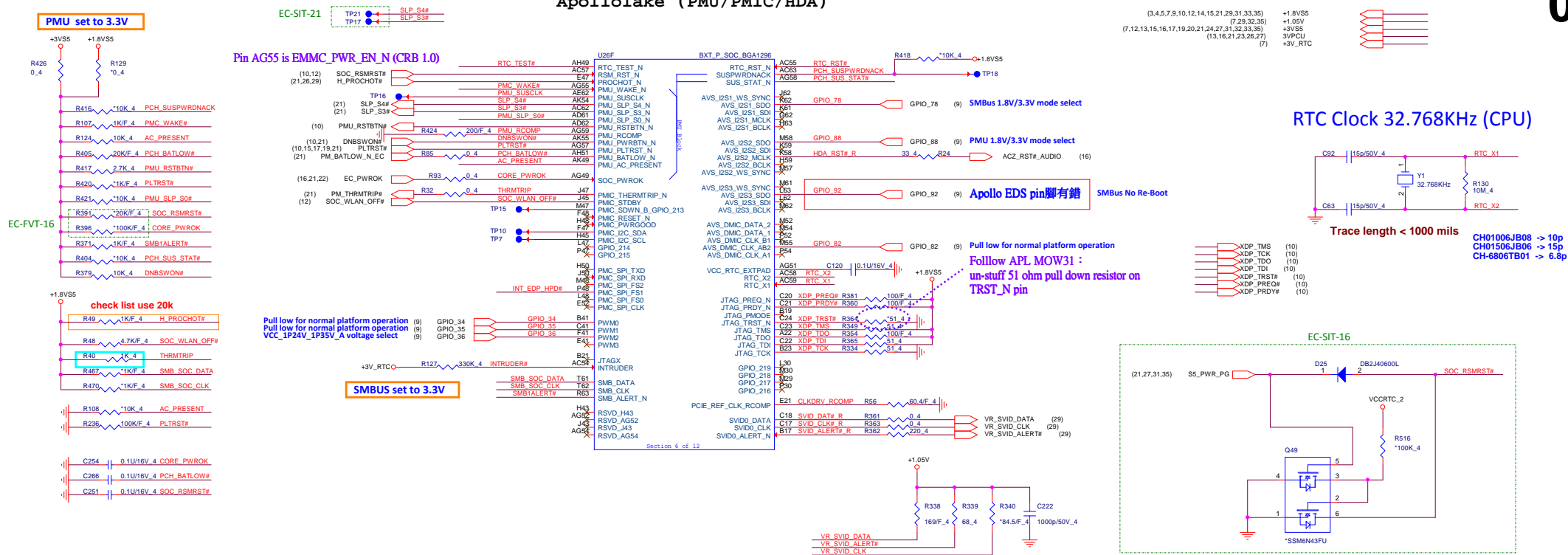


<1000 mil

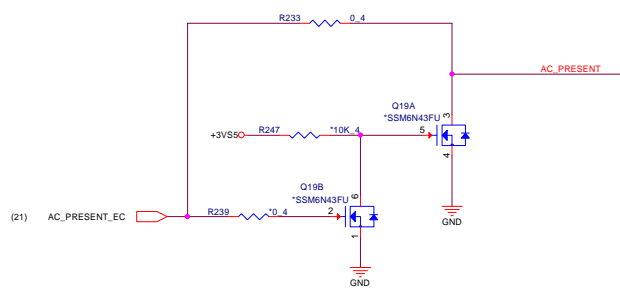


PROJECT : LI8G
Quanta Computer Inc.

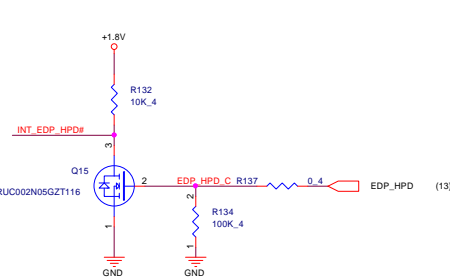
Apollolake (PMU/PMIC/HDA)



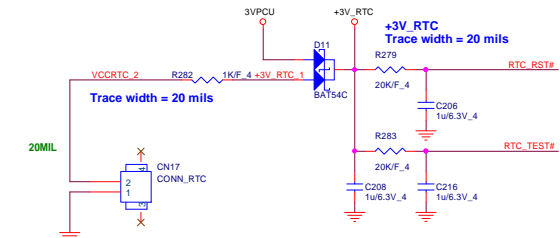
AC_PRESENT



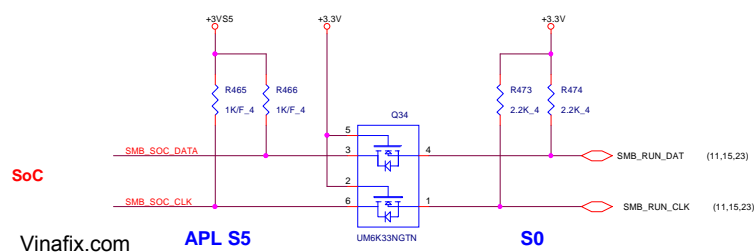
eDP HPD



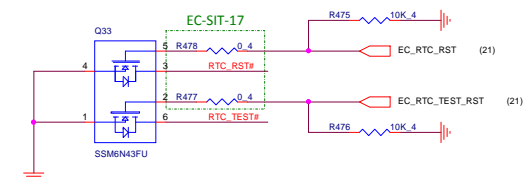
RTC Circuitry (RTC)



SMBus



DDR3L
Click Pad



+VNN Output Decoupling Recommendations

1uF3	0402	BOT, inside socket cavity
22uF4	0603	TOP, inside socket cavity

VDD2_1P24_GLM_L Output Decoupling Recommendations

1uF3	0402	TOP*1 / BOT*3, inside socket cavity
22uF1	0603	TOP, inside socket cavity

VDD2_1P24_DSI_CSI Output Decoupling Recommendations

1uF2	0402	TOP*1 / BOT*1, inside socket cavity
22uF1	0603	TOP, inside socket cavity

VDD2_1P24_AUD_ISH_PLL Output Decoupling Recommendations

1uF2	0402	TOP*1 / BOT*1, inside socket cavity
22uF1	0603	TOP, inside socket cavity

VDD2_1P24_MPHY Output Decoupling Recommendations

1uF3	0402	TOP*1 / BOT*2, inside socket cavity
22uF1	0603	TOP, inside socket cavity

VCCRAM_1P05_IO_3PHASEIO Output Decoupling Recommendations

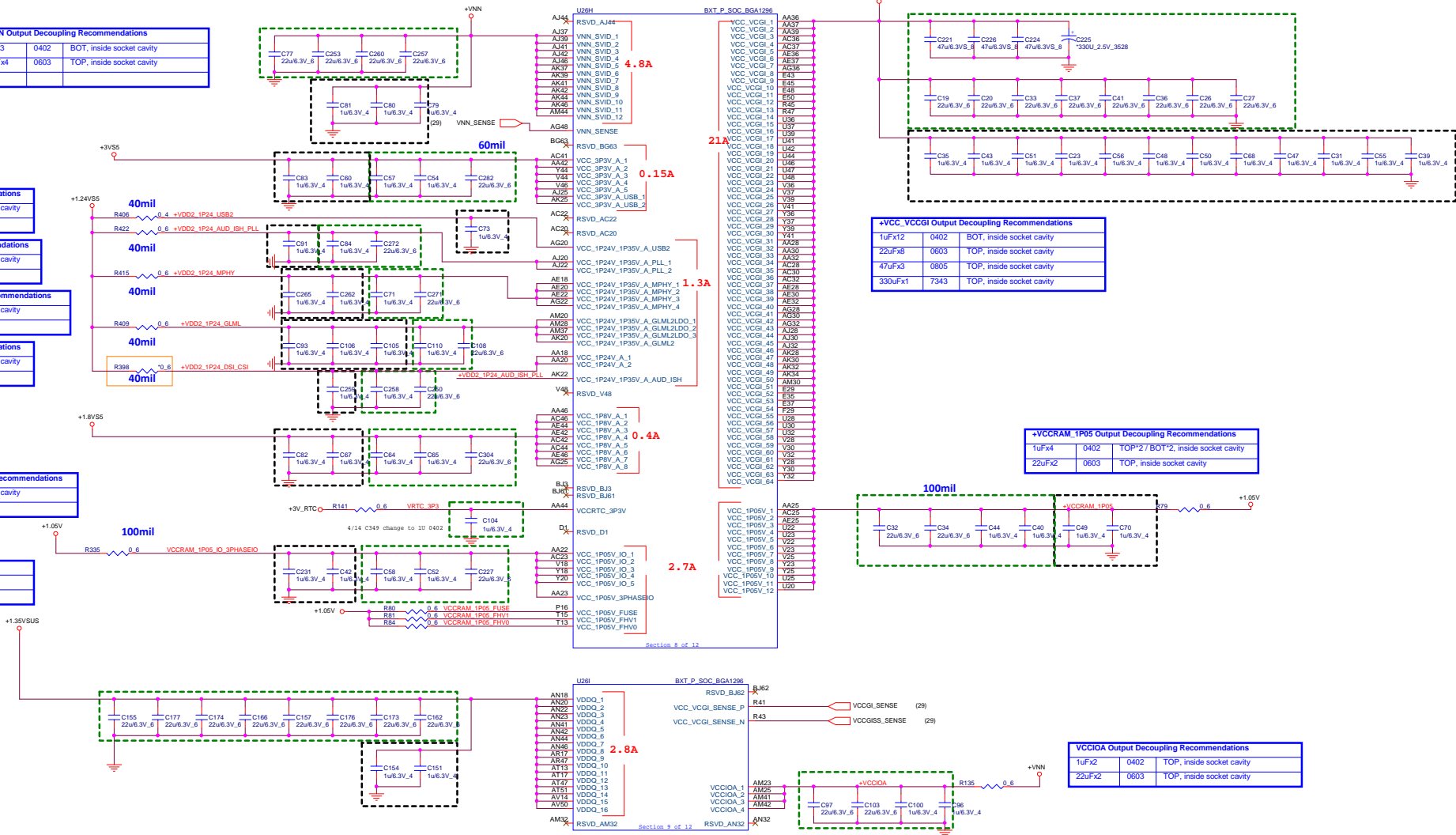
1uF4	0402	TOP*2 / BOT*2, inside socket cavity
22uF1	0603	TOP, inside socket cavity

+VCCDDQ Output Decoupling Recommendations

1uF2	0402	BOT, inside socket cavity
22uF8	0603	TOP, inside socket cavity

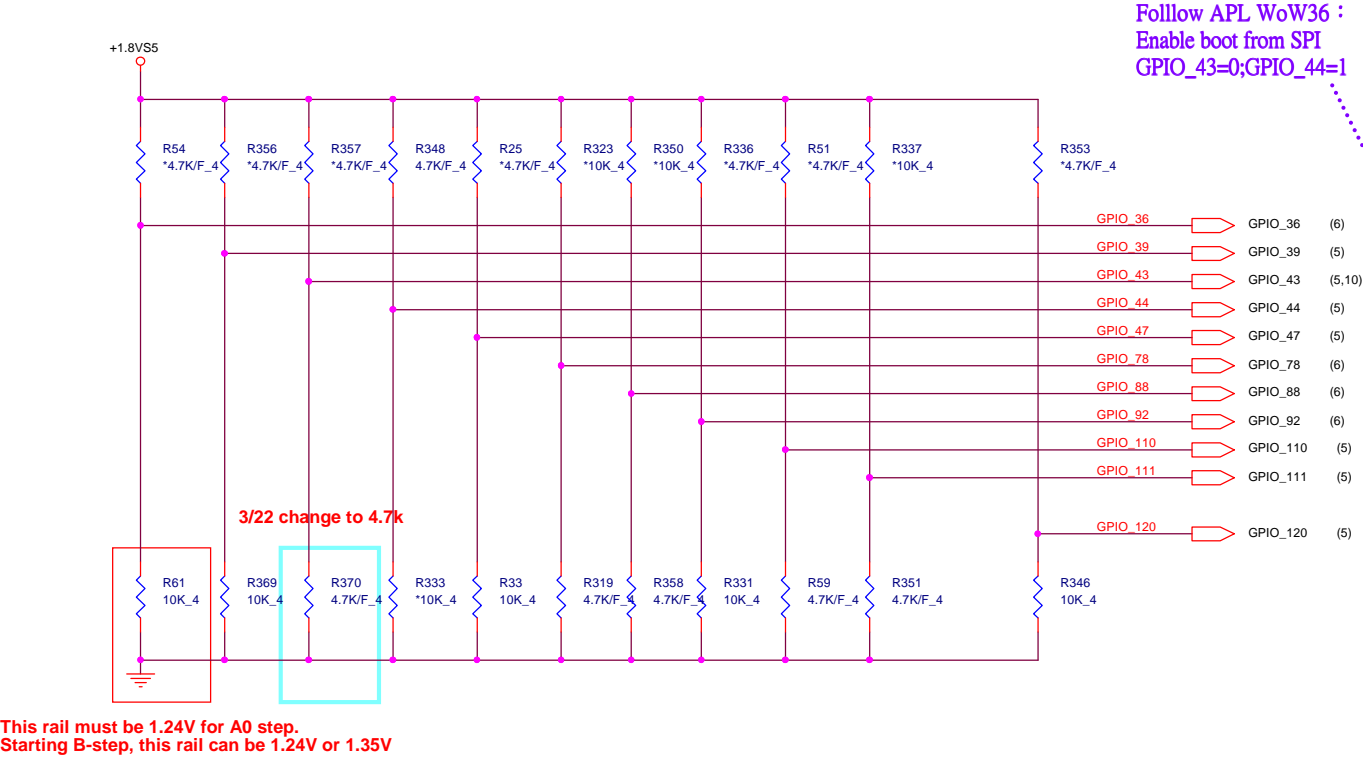
VCCIOA Output Decoupling Recommendations

1uF2	0402	TOP, inside socket cavity
22uF2	0603	TOP, inside socket cavity



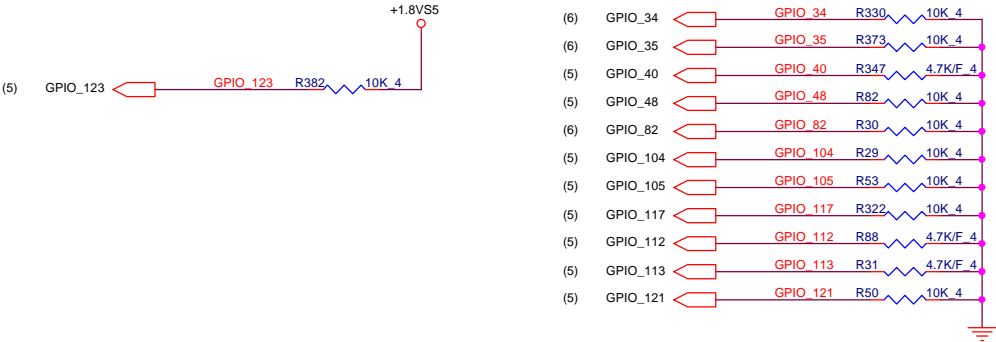
PROJECT : L18G
Quanta Computer Inc.

Size Document Number
BXT_P (POWER)
Date: Thursday, September 08, 2016 Sheet 7 of 40



(3,4,5,6,7,10,12,14,15,21,29,31,33,35) +1.8VS5

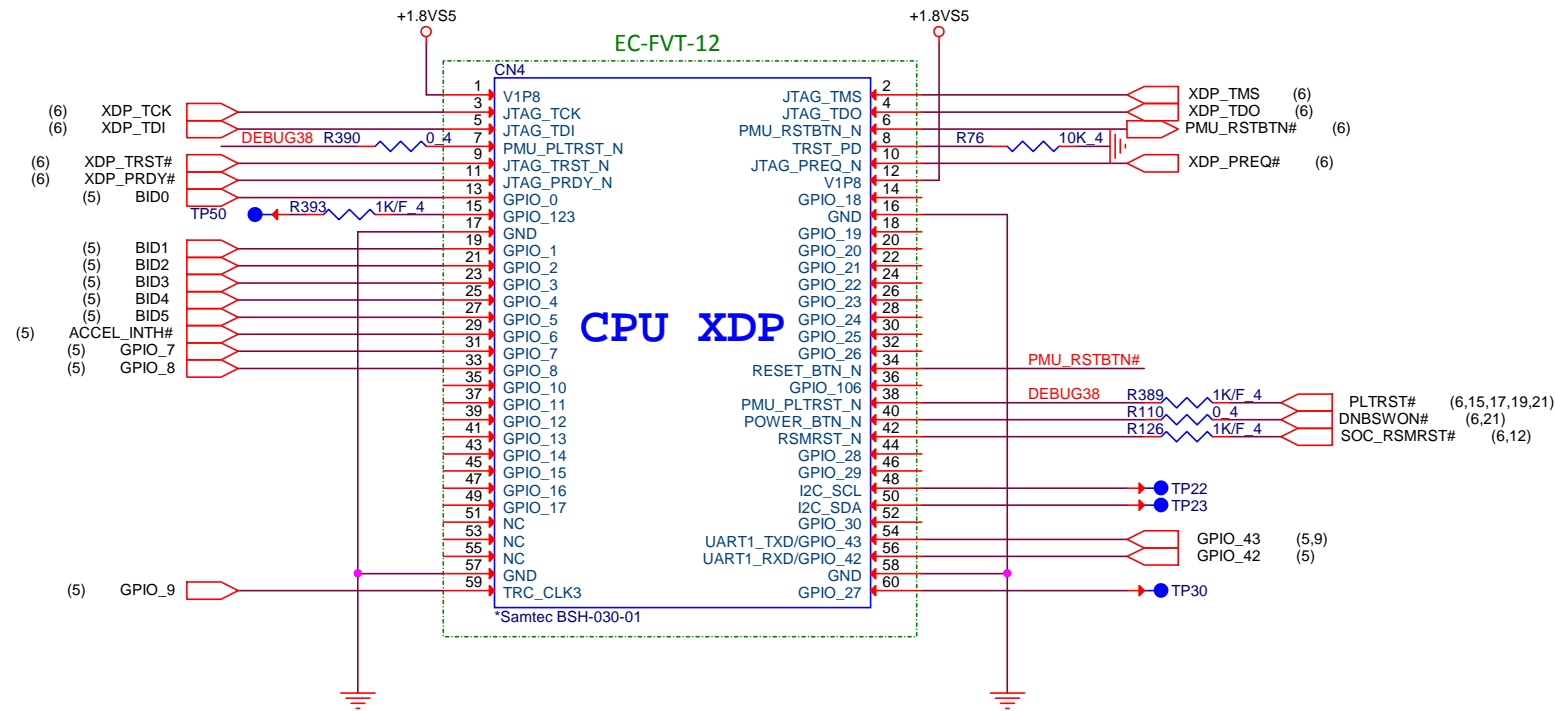
Hardware Strap	Strap Description	Value
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V	0
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass	0
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable	0
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable	1
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force	0
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V	0
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI	0
GPIO_120	Top swap override 0 = Disable 1 = Enable	0



Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_40/GPIO_48/GPIO_104/GPIO_105/GPIO_112/GPIO_113/GPIO_117/GPIO_121 PD
GPIO_106/GPIO_123 PU

(3,4,5,6,7,9,12,14,15,21,29,31,33,35)

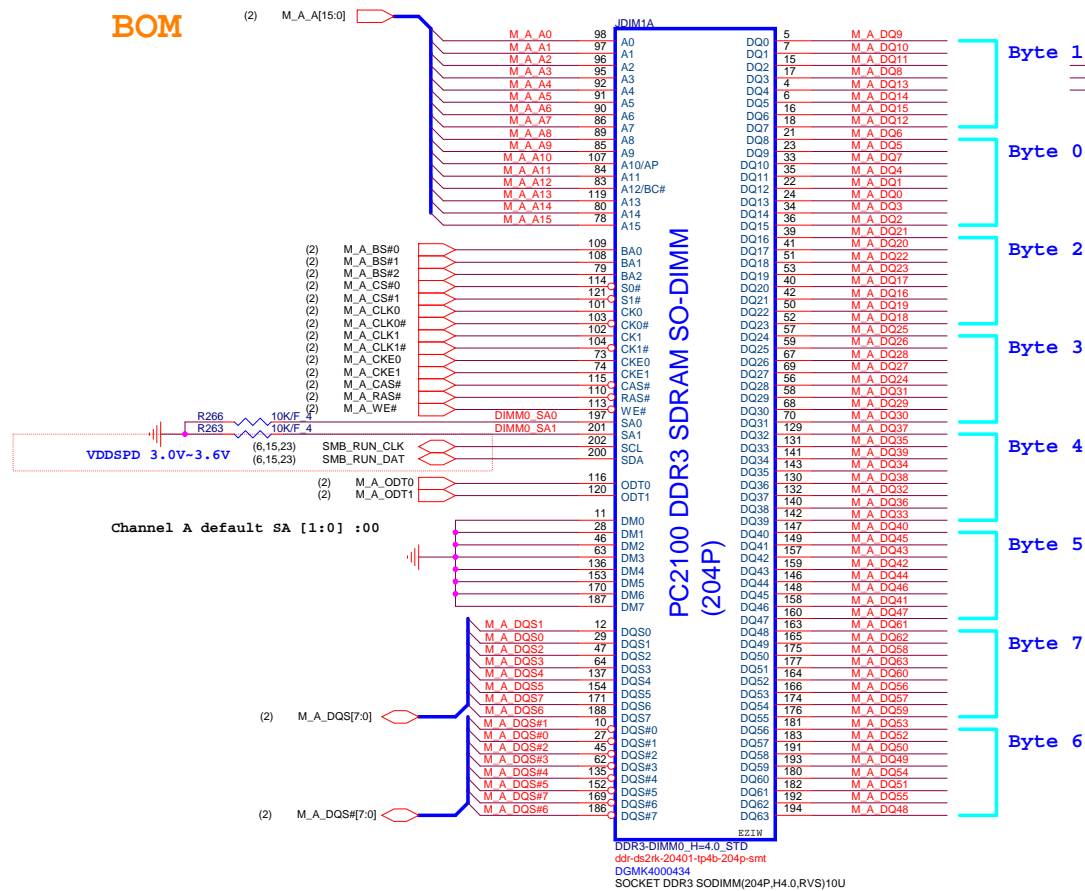
+1.8VS5



PROJECT : LI8G
Quanta Computer Inc.

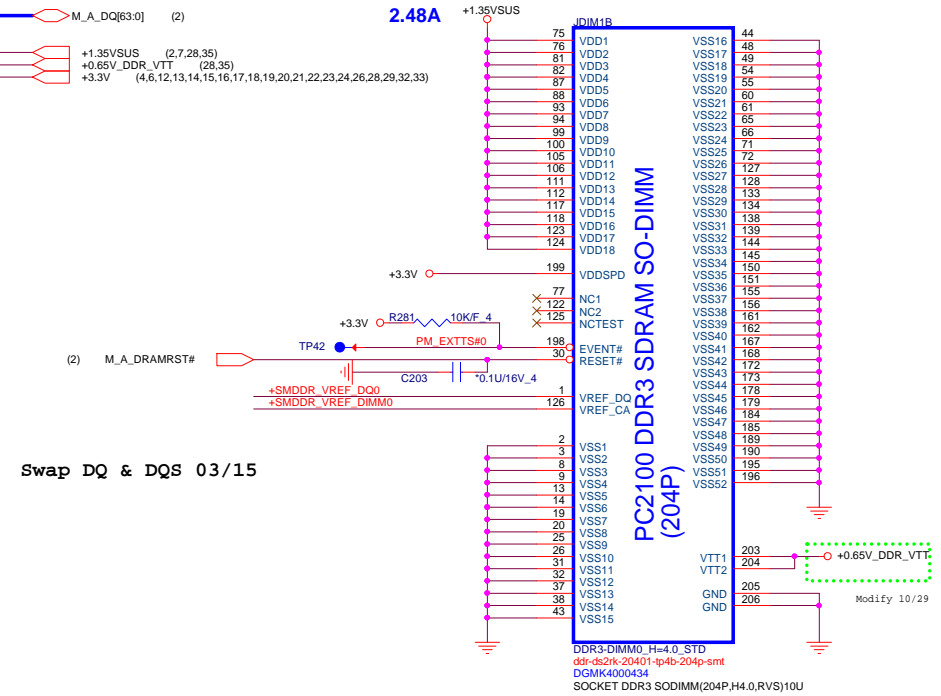
Size	Document Number	Rev
	APL XDP	1A
Date:	Thursday, September 08, 2016	Sheet 10 of 40

BOM

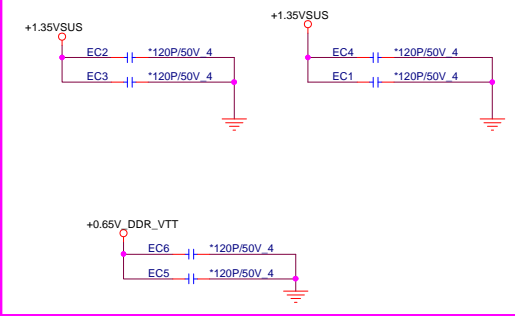


Swap DQ & DQS 03/15

2.48A

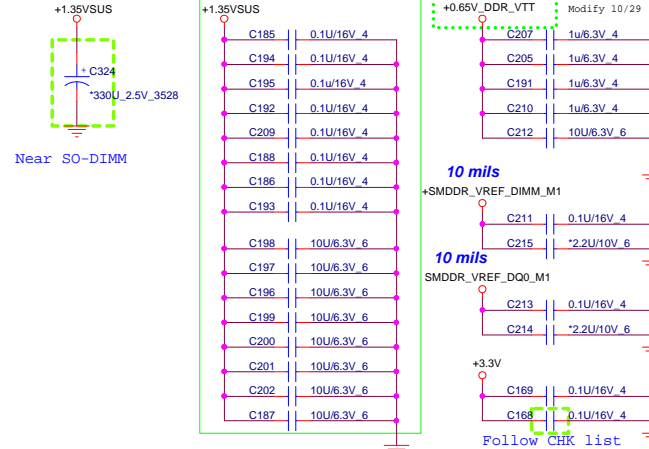


For EMI RESERVE

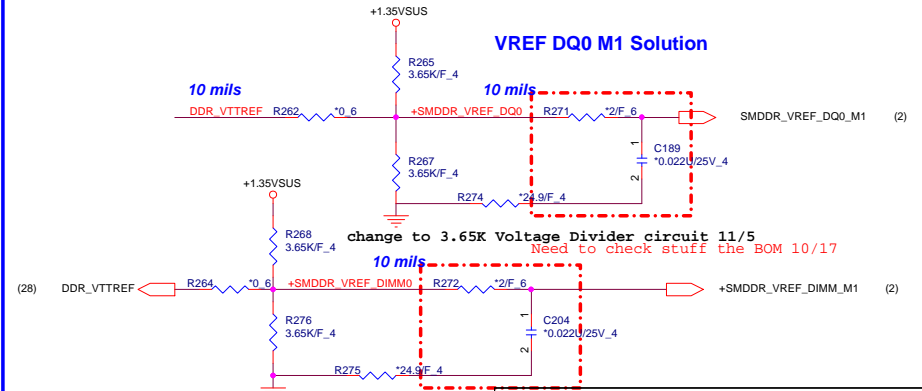


Place these Caps near So-Dimm0.

0.1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution



Correct CHA VREF_DQ/CA net name 10/29

PROJECT : LI8G

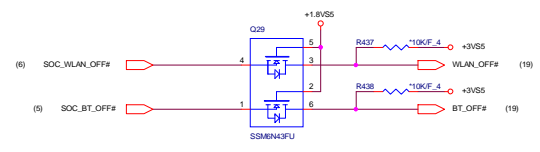
Quanta Computer Inc.

Size Document Number

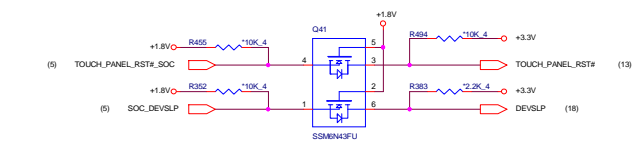
DDR3L DIMM0-RVS(4.0H)CH-A

Date: Thursday, September 08, 2016 Sheet 11 of 40

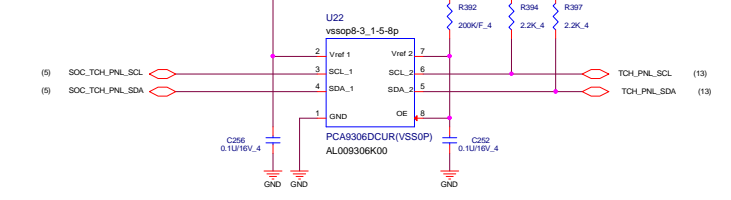
RF OFF#



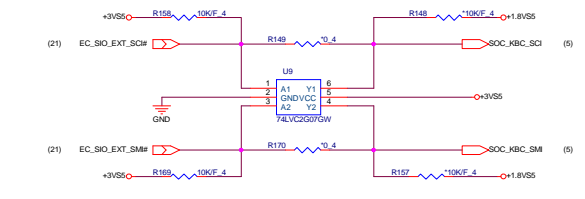
TCH_RST#/DEVSLP



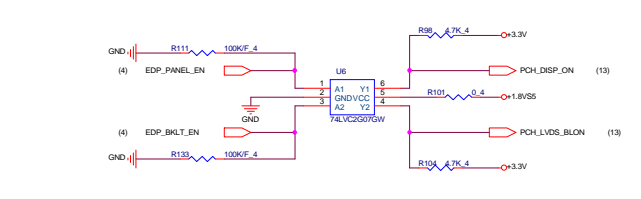
Touch Panel I2C(OK)



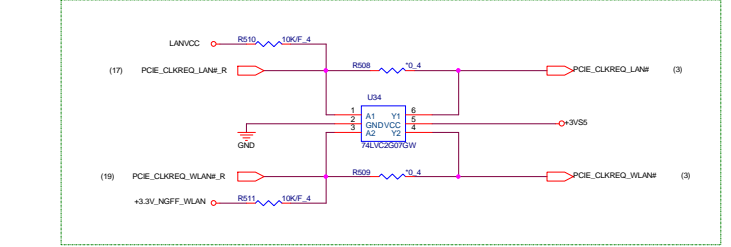
SCI#/SMI#(OK)



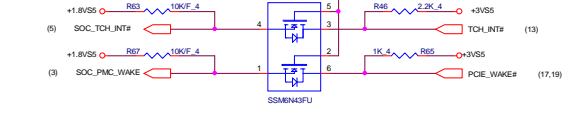
Disp ON/BL ON(OK)



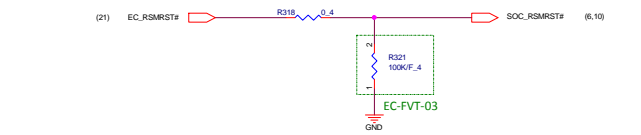
CLKREQ#



INT



RSMRST#(OK)



PROJECT : LI8G

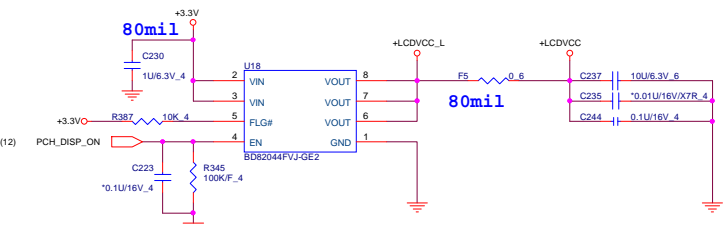
Quanta Computer Inc.

Size Document Number Rev 1A

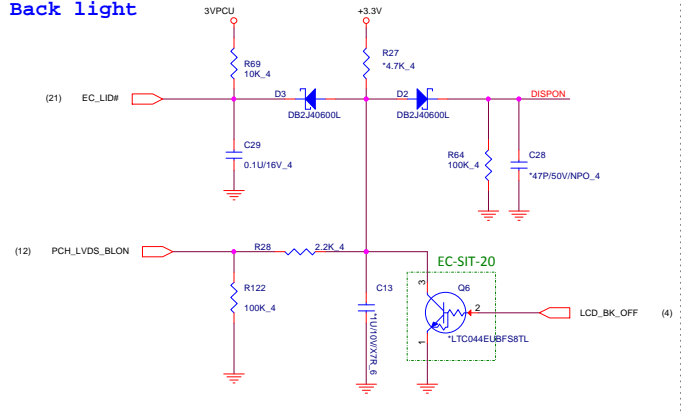
Level shift/Thermistor

Date: Thursday, September 08, 2016 Sheet 12 of 40

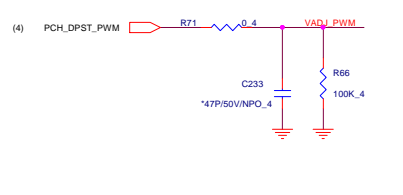
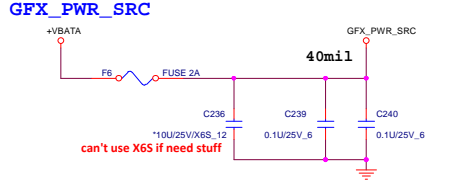
LCDVCC



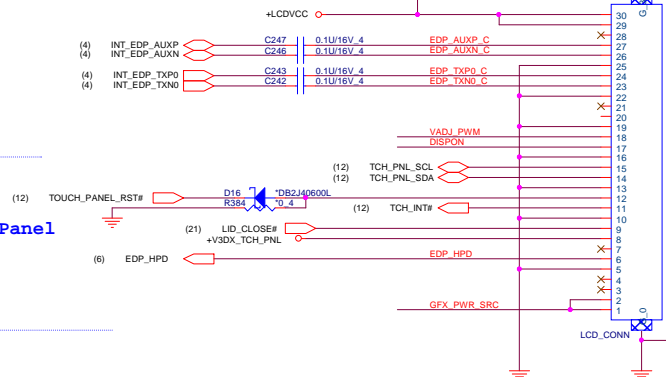
Back light



GFX_PWR_SRC

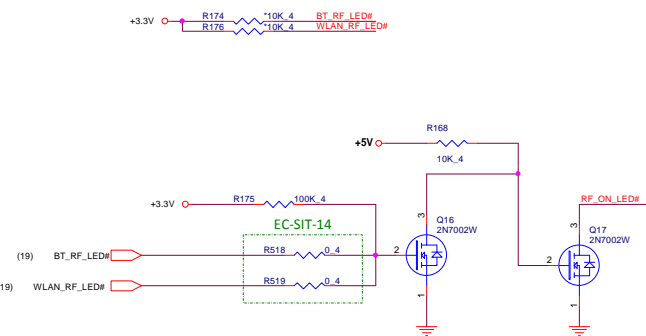
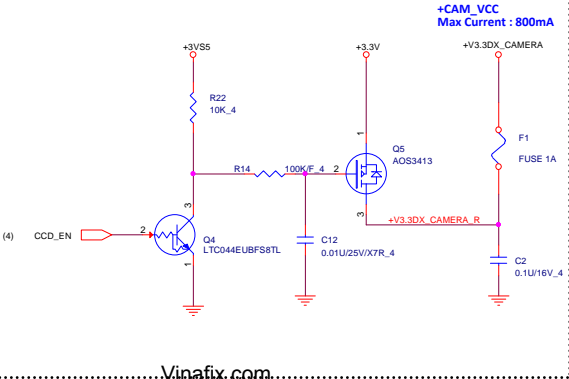


Touch Panel

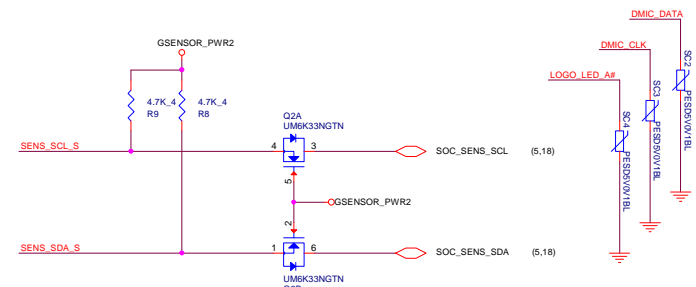
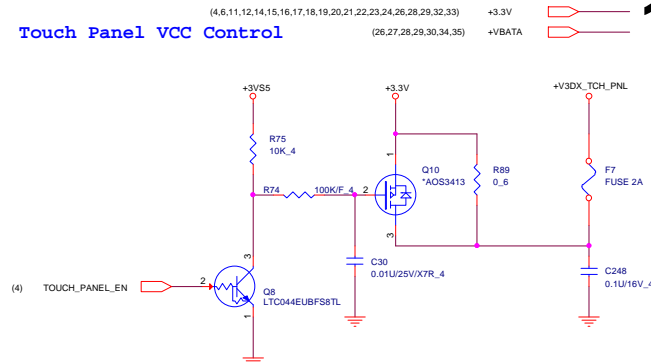


CCD+MIC+LOGO+WLAN LED CONN

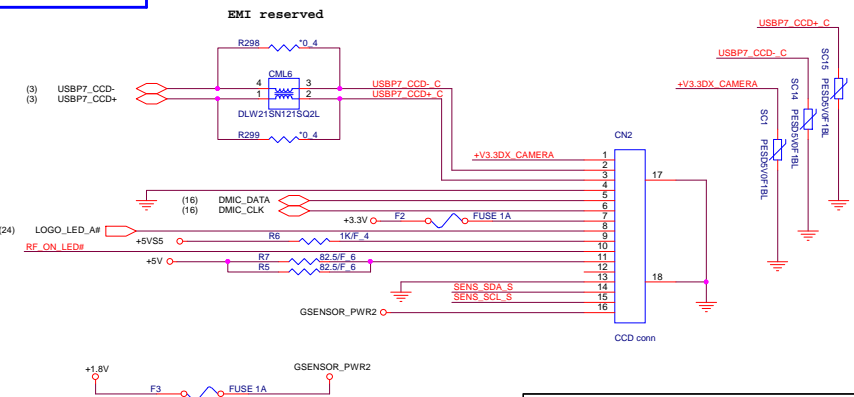
CAMERA VCC Control

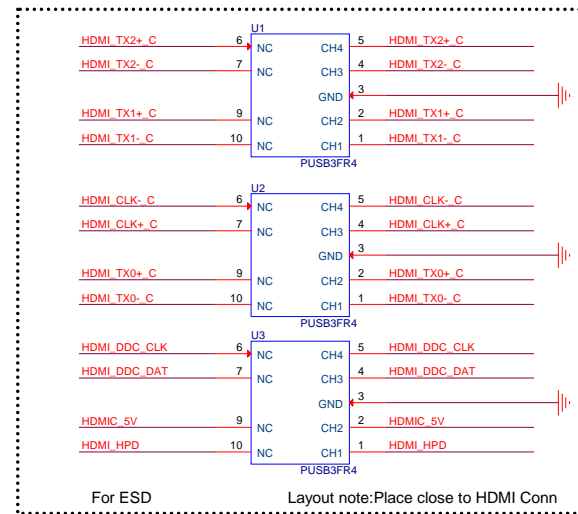
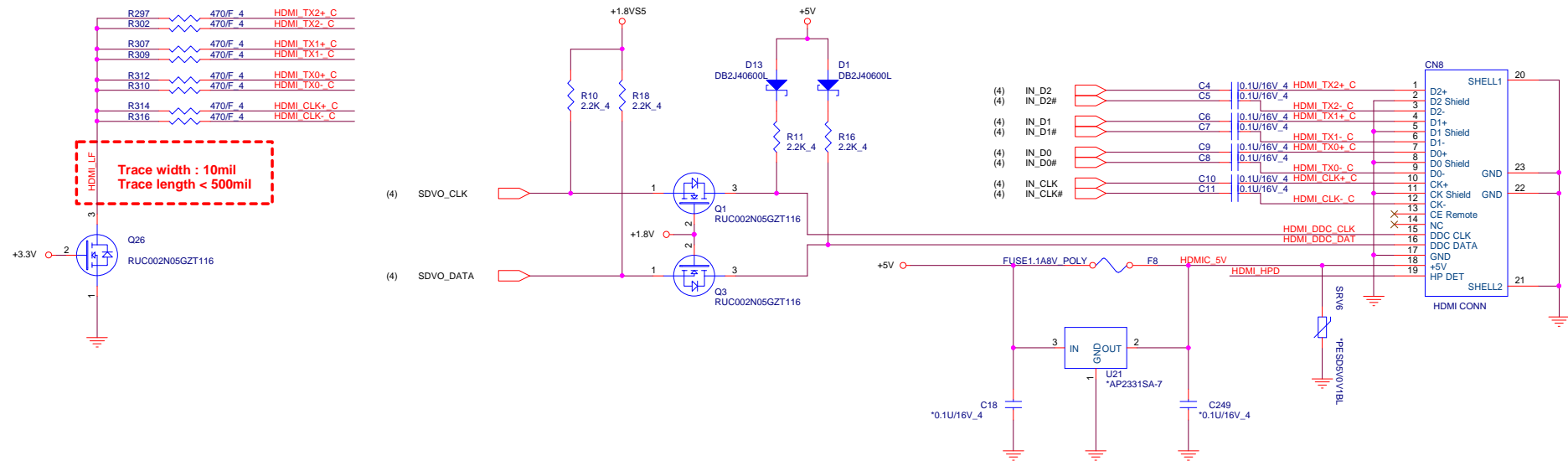


Touch Panel VCC Control

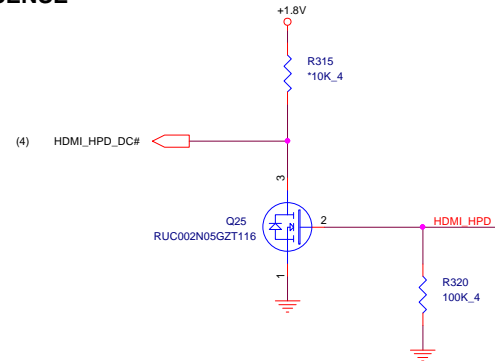


EMI reserved



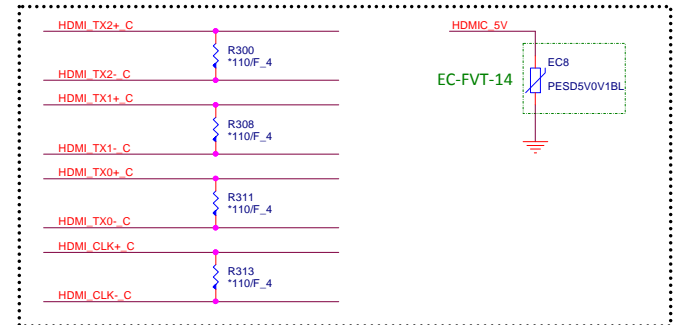


HDMI HPD SENSE



Note: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage $\leq 1.5V$.
Note: It's required to enable internal 20K PU resistor on these HV_DDIx_HPDI signals by BIOS

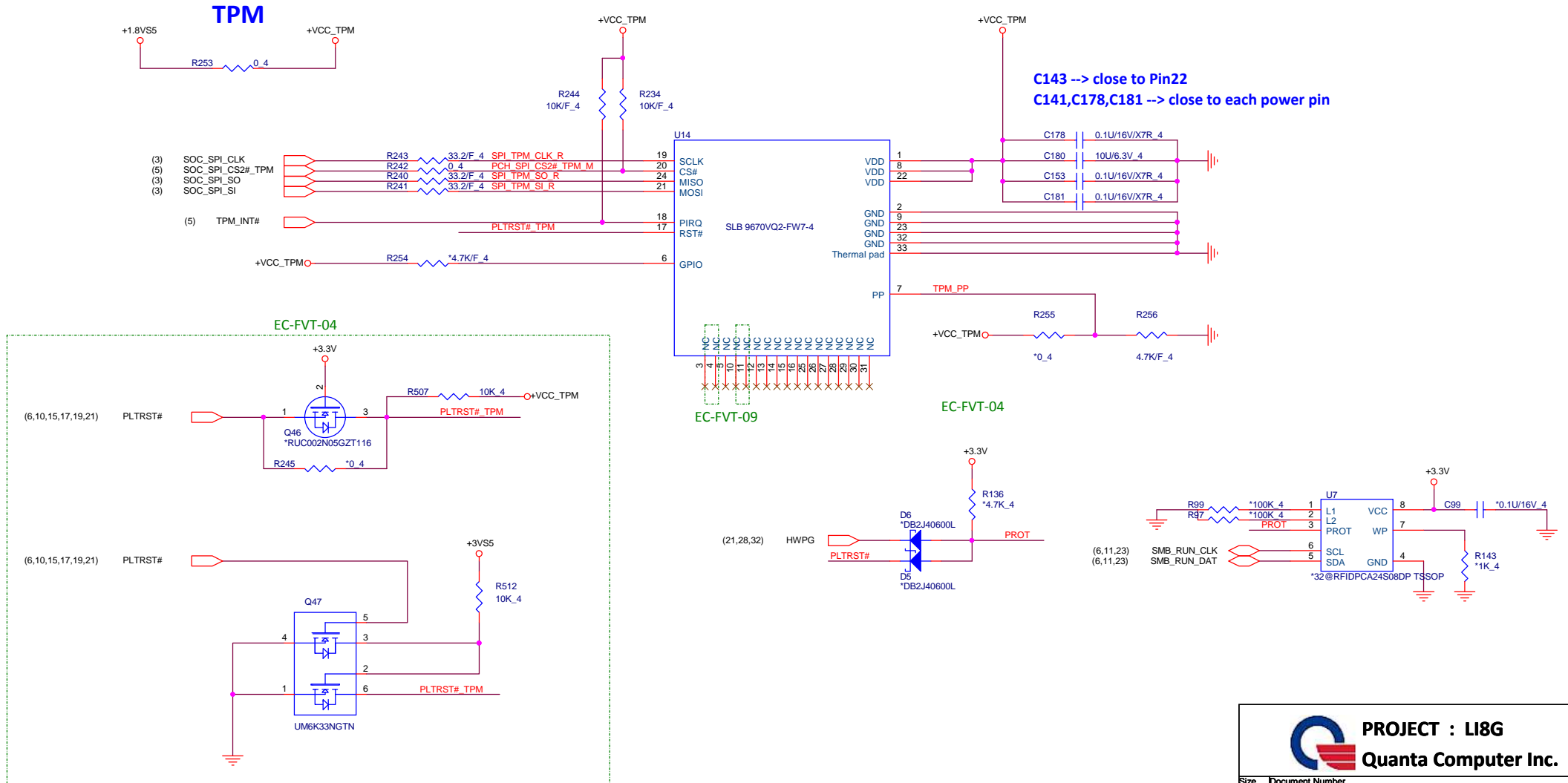
EMI reserve for HDMI



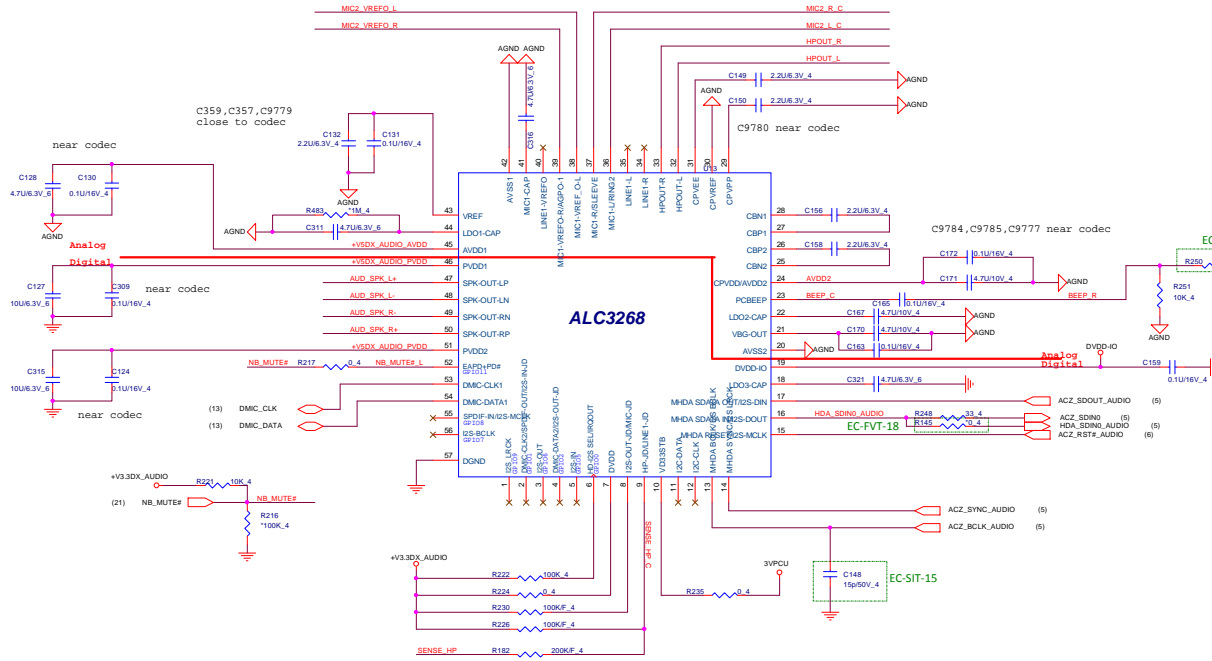
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI CONN	1A
Date:	Thursday, September 08, 2016	Sheet 14 of 40

HDMI CONN



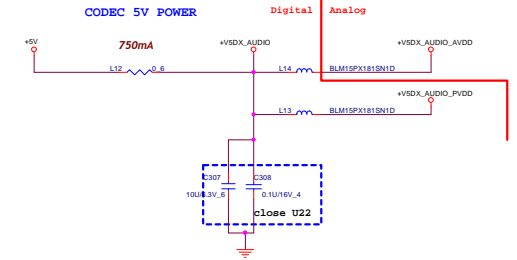
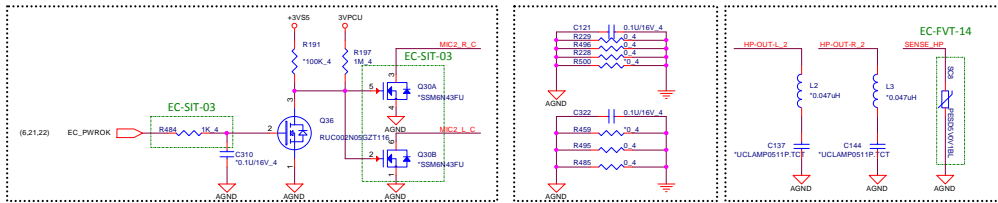
ALC3268



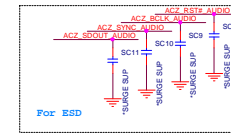
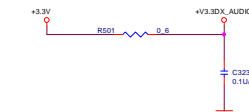
ALC3268

External MIC/ Headphone out combo

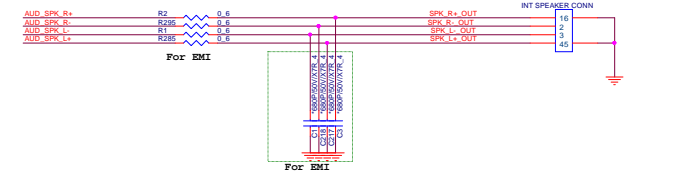
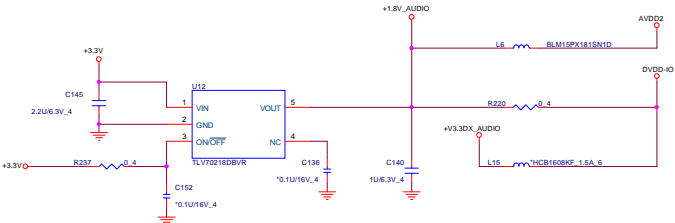
Grounding circuit for combo jack MIC R/L pin



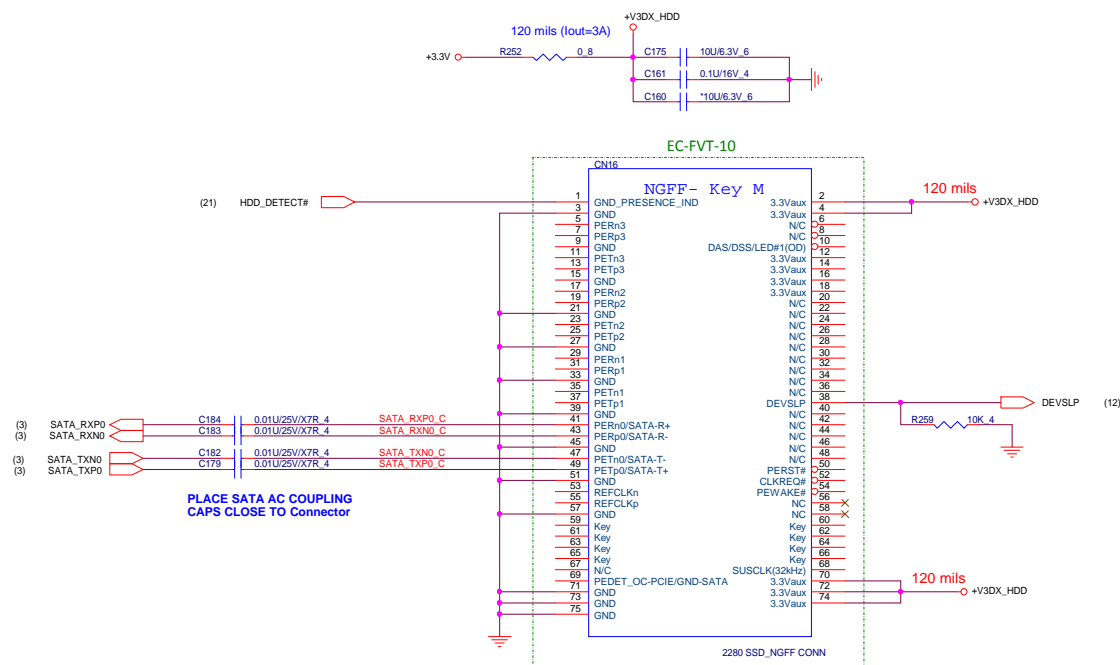
+3.3V AUDIO CODEC
Max Current : 419mA



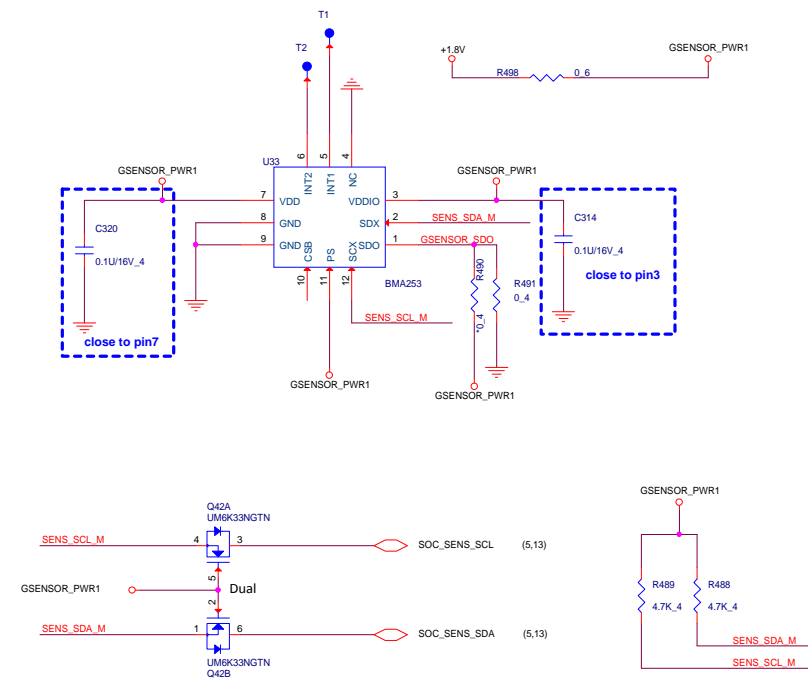
INT Speaker



DC Current rating: 3 A (MAX)



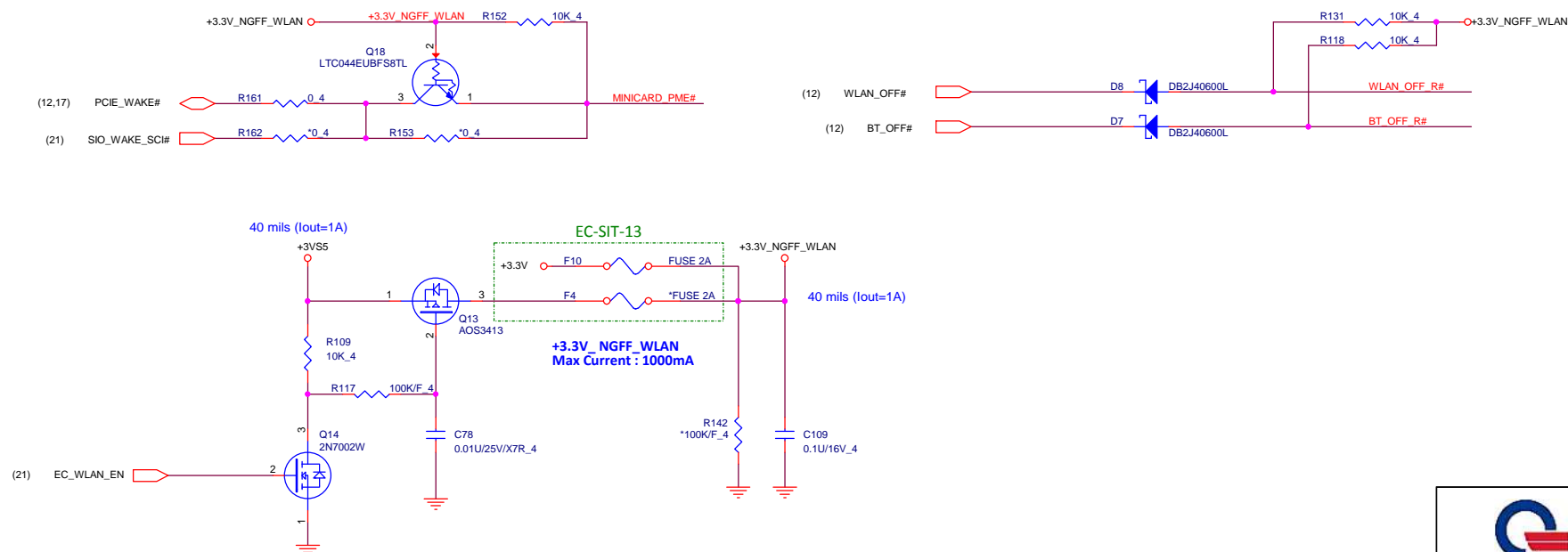
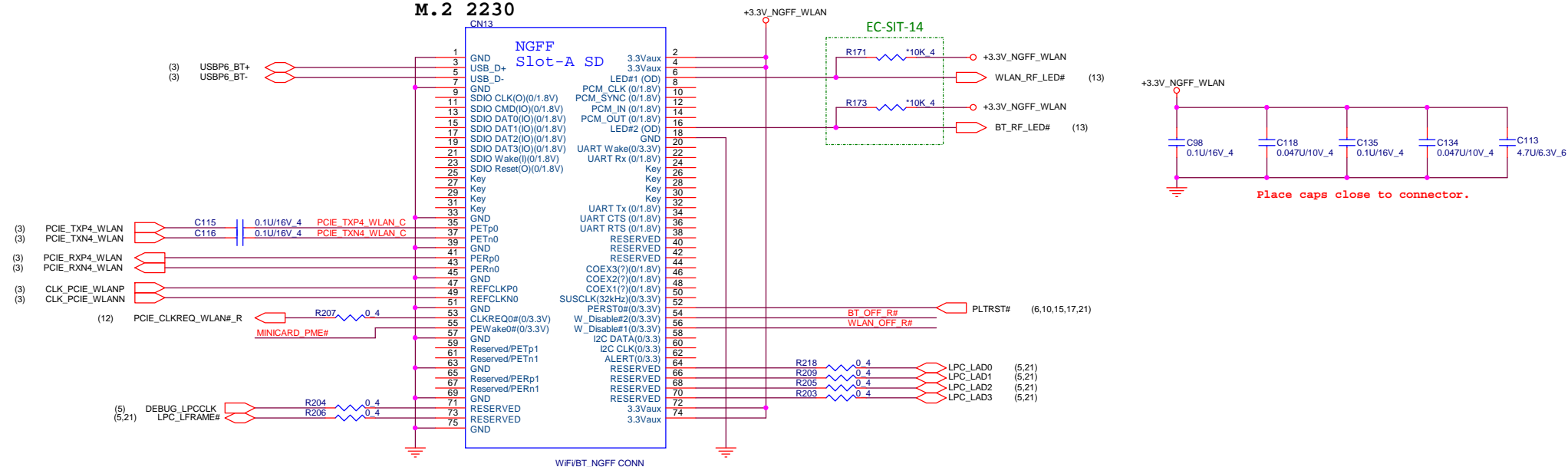
G-SENSOR For Yoga



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	M.2 2280/G-SENSOR	1A
Date:	Thursday, September 08, 2016	Sheet 18 of 40

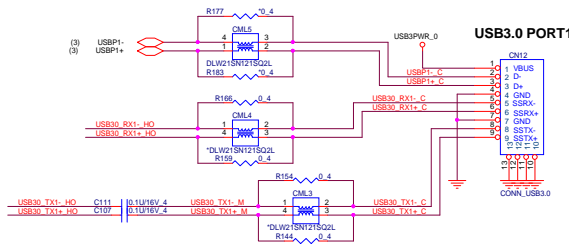
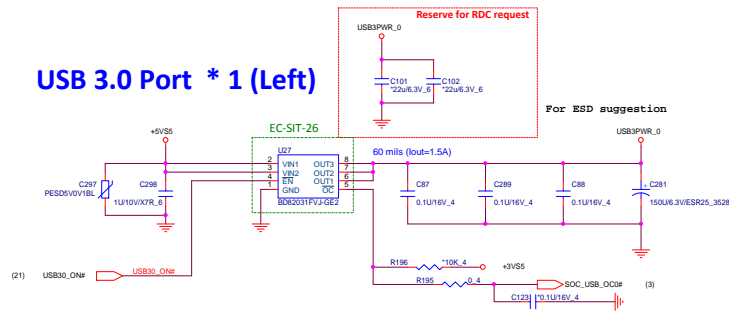
NGFF WiFi/BT connector M.2 2230



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	WIFI/BT NGFF	1A
Date:	Thursday, September 08, 2016	Sheet 19 of 40

USB 3.0 Port * 1 (Left)



For ESD

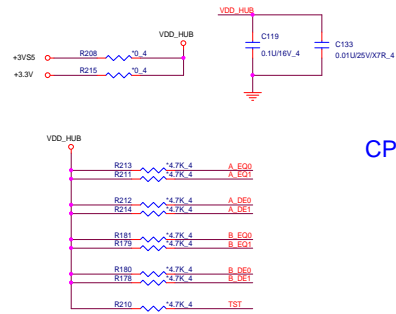


By pass shortcut

CPU

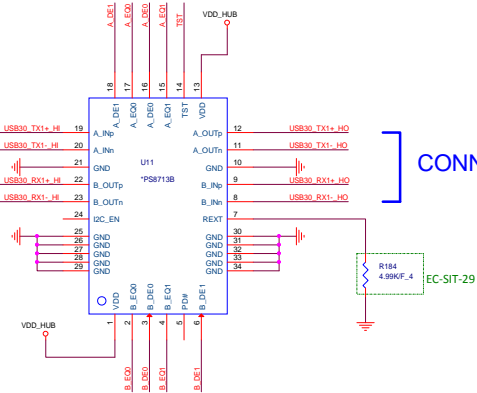
CONN

USB 3.0 Redriver (Reserved)

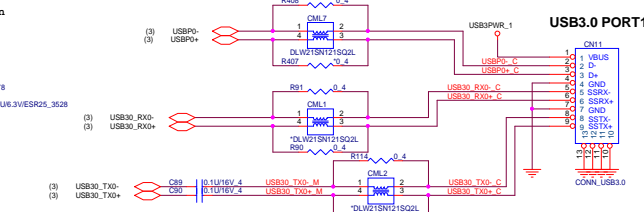
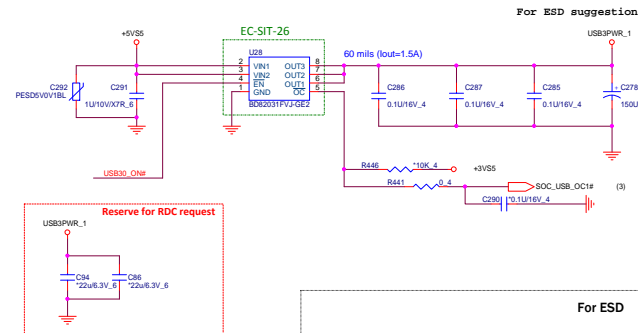


CPU

CONN



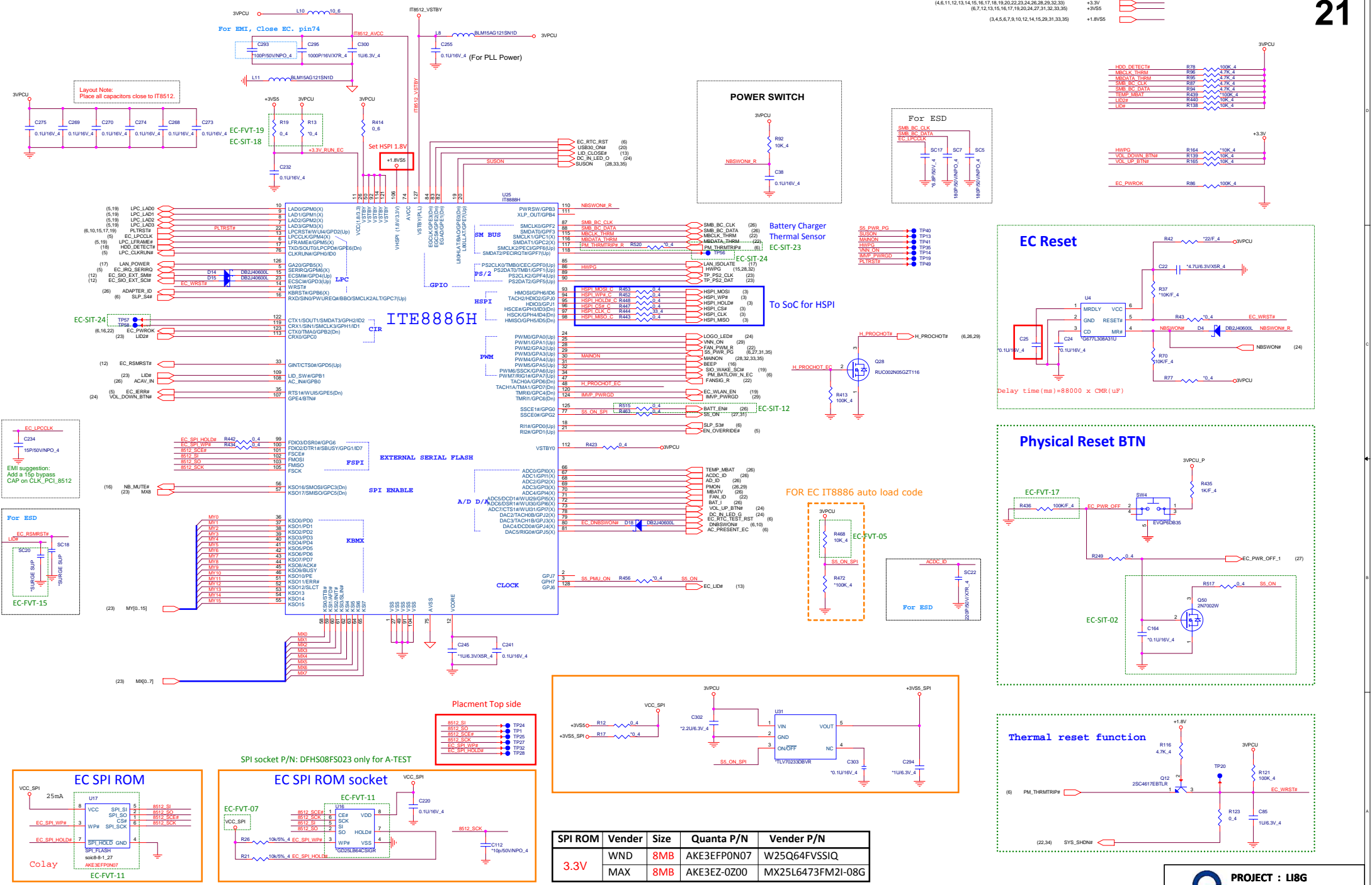
USB 3.0 Port * 1 (Right)



For ESD



Vinafix.com



SPI ROM	Vender	Size	Quanta P/N	Vender P/N
3.3V	WND	8MB	AKE3EFP0N07	W25Q64FVSSIQ
	MAX	8MB	AKE3EZ-0Z00	MX25L6473FM2I-08G

PROJECT : LI8G
Quanta Computer Inc.

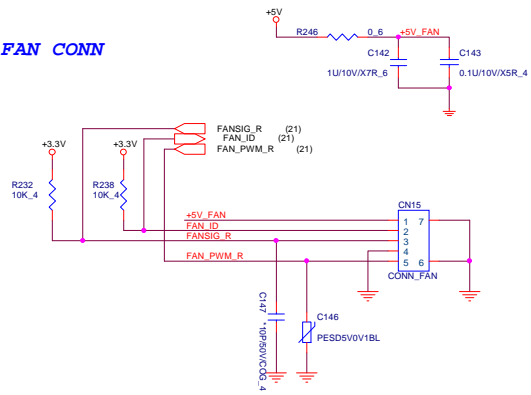
Doc: **KBC IT8886**

Date: **Friday, September 06, 2016**

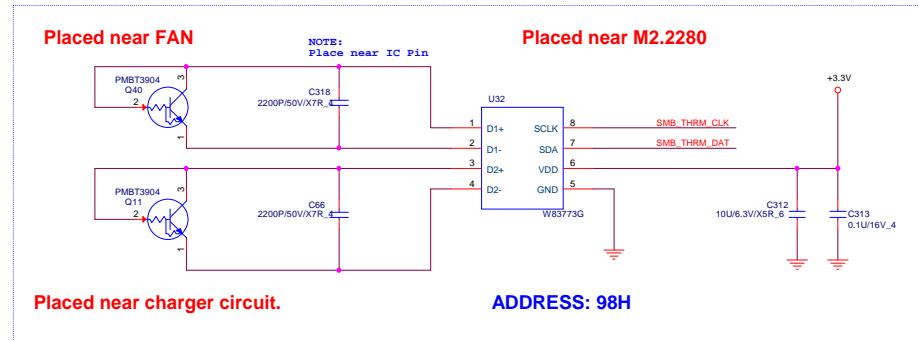
Rev: **1A**

Sheet: **21** of **40**

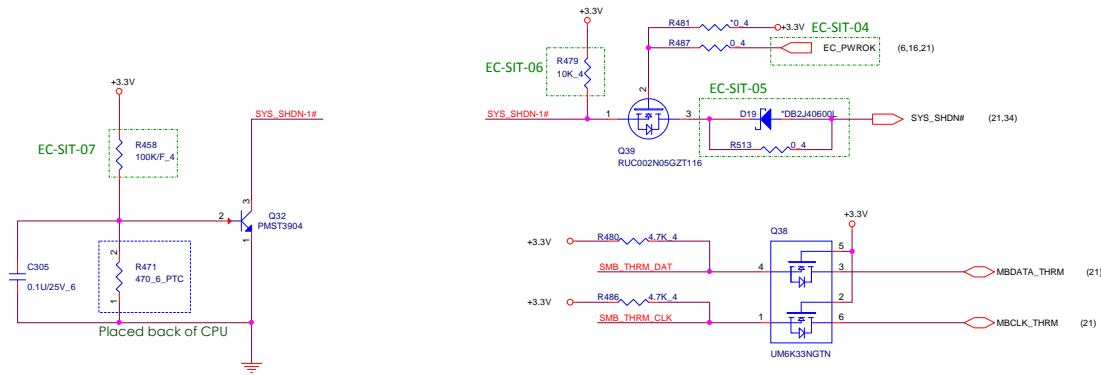
FAN CONN



Thermal Sensor



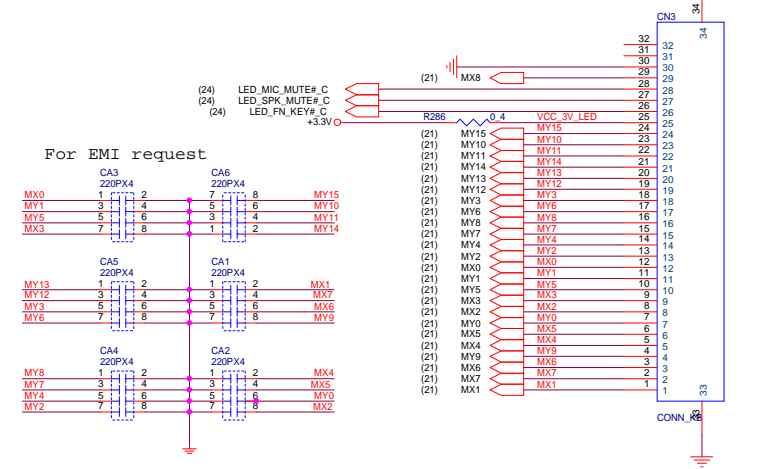
CPU PTC circuit



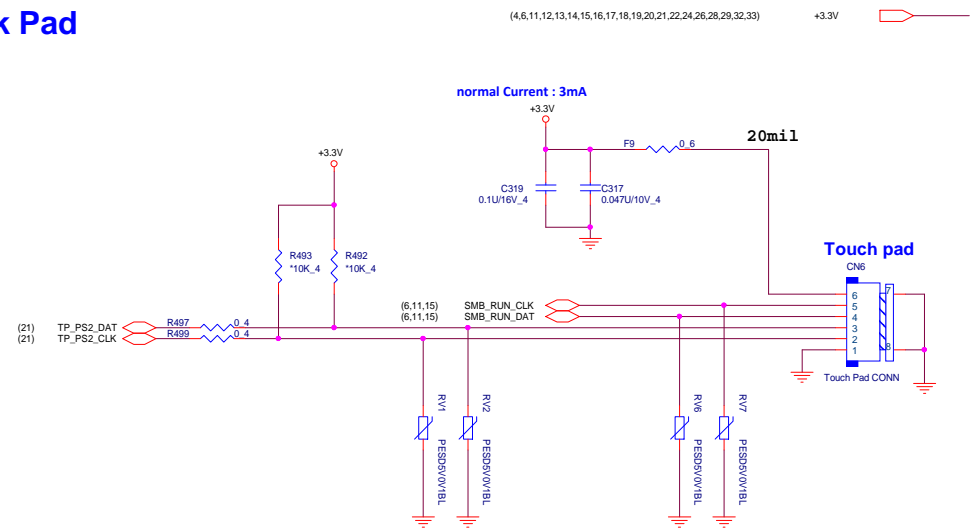
To EC

PROJECT : LI8G		
Quanta Computer Inc.		
Size	Document Number	Rev
	FAN/Thermal	1A
Date	Thursday, September 08, 2016	Sheet 22 of 40

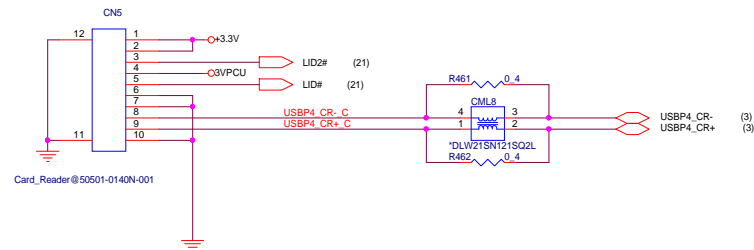
KEYBOARD



Click Pad



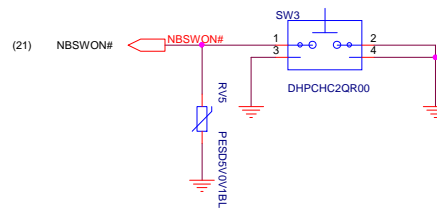
To Card Reader Board



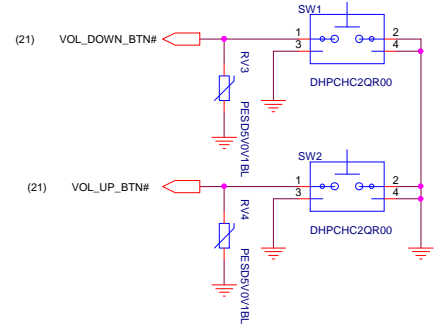
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/DB	1A
Date: Thursday, September 08, 2016	Sheet 23 of 40	

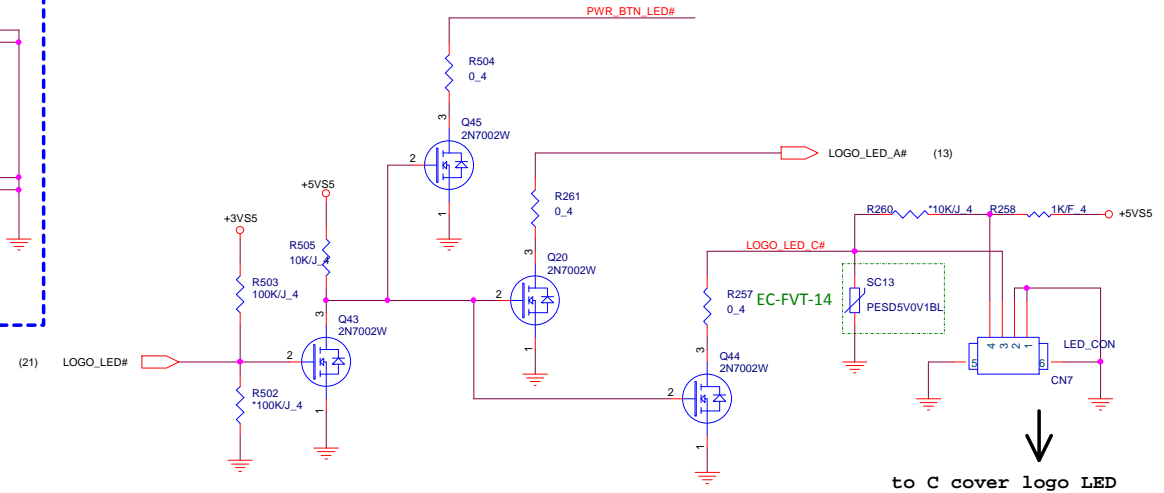
Power Switch



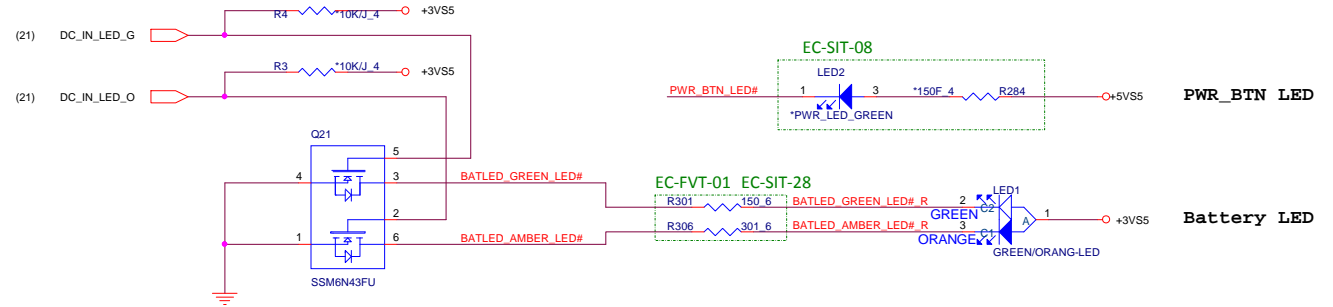
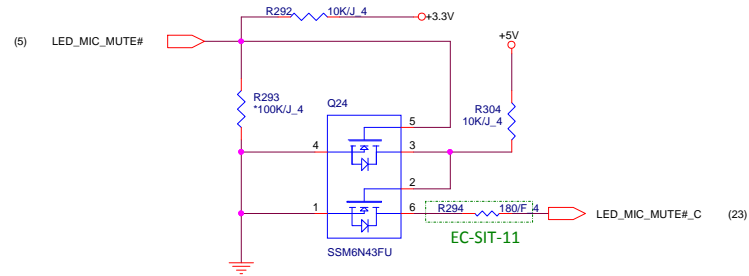
Volume up/down Switch



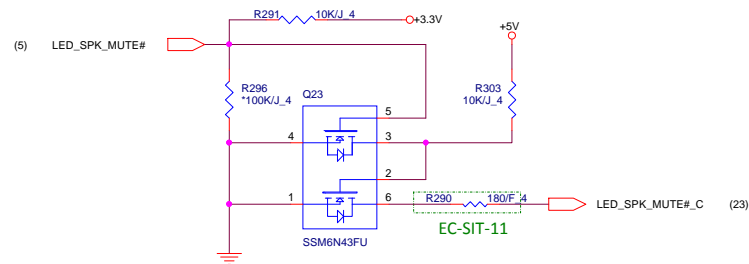
A/C cover & power button LED



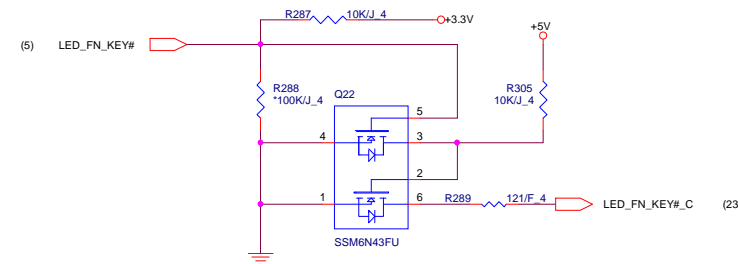
Mute LED



Speaker LED

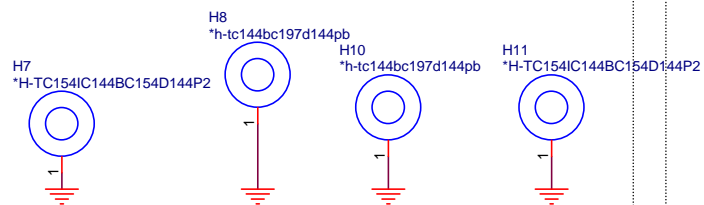
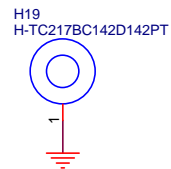
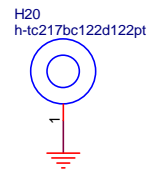
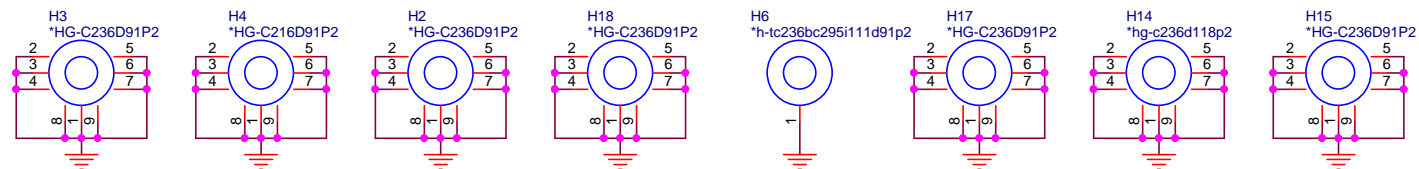
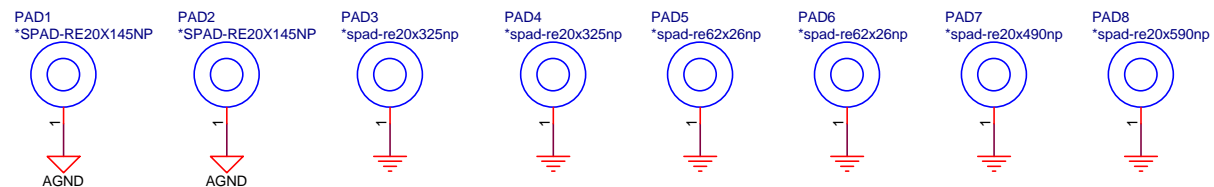


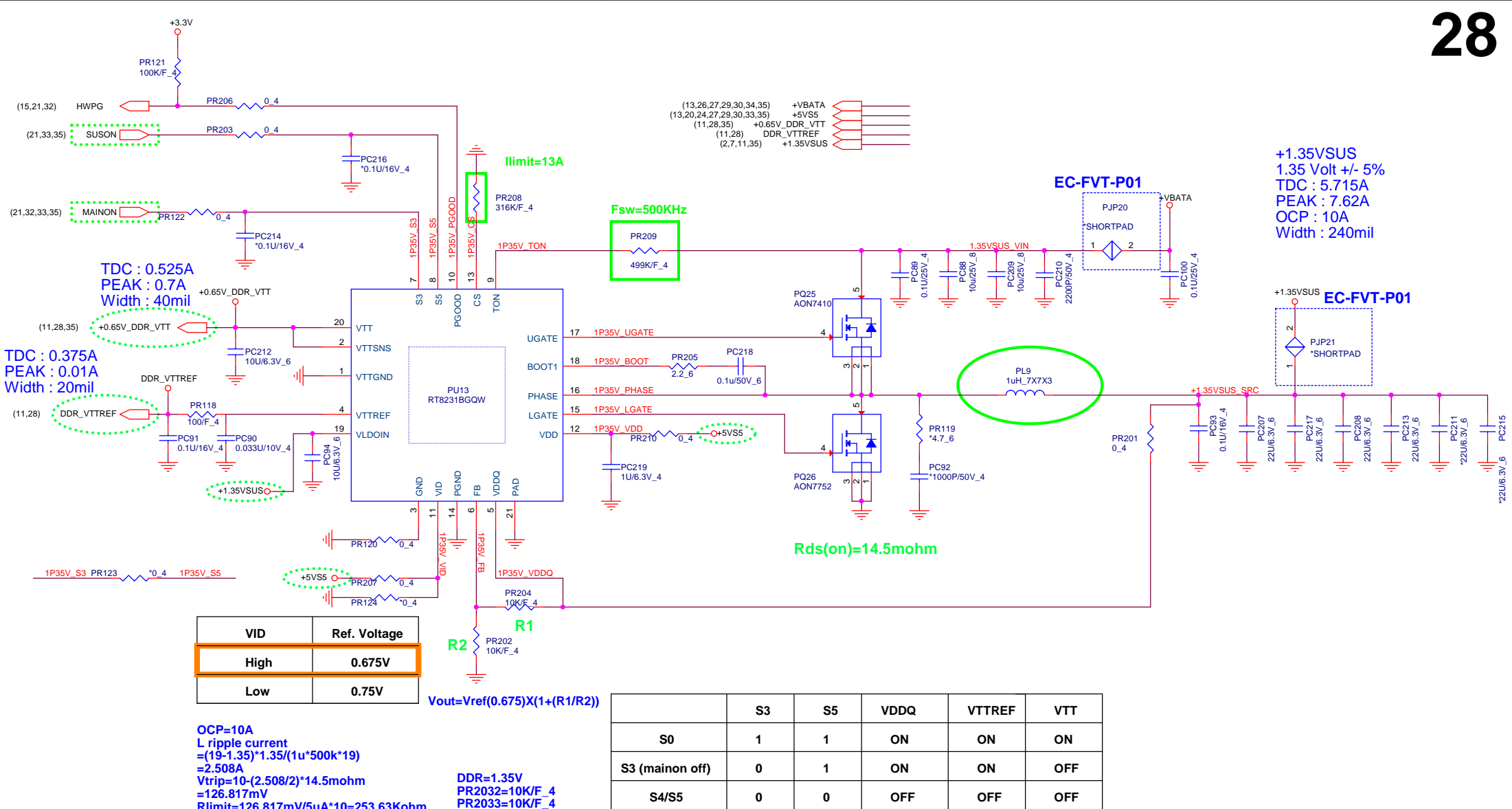
Fn key LED




PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/SW	1A
Date:	Monday, September 12, 2016	Sheet 24 of 40

Hole For CPU bracket**NGFF WLAN****NGFF M.2 2280****Boundary Hole****PAD****Non-PTH Hole**





PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	DDR(RT8231BGQW)	1A
Date:	Thursday, September 08, 2016	Sheet 28 of 40

SVID_CLK : UP:85 ohm Series:95 ohm
 SVID_ALERT : UP:68 ohm Series:220 ohm
 SVID_DATA : UP:170 ohm Series:20 ohm

Change pull up to +1.05V_S5

IMVP8 VR Controller

Rail A (1 phase) : +VCCGI

Rail C (1 phase) : +VNN

可能缺料

Modify 10/30

Add s5_ON for VNN sequence
 Check VR Sequence

Double Check Rail B Non-Usage Pin

APL VR (1+1 Phase)

+VCCGI

Icc Max : 21A
 Icc TDC : 18A
 Vboot : 0V
 OCP : 25A
 Fsw : 750KHZ

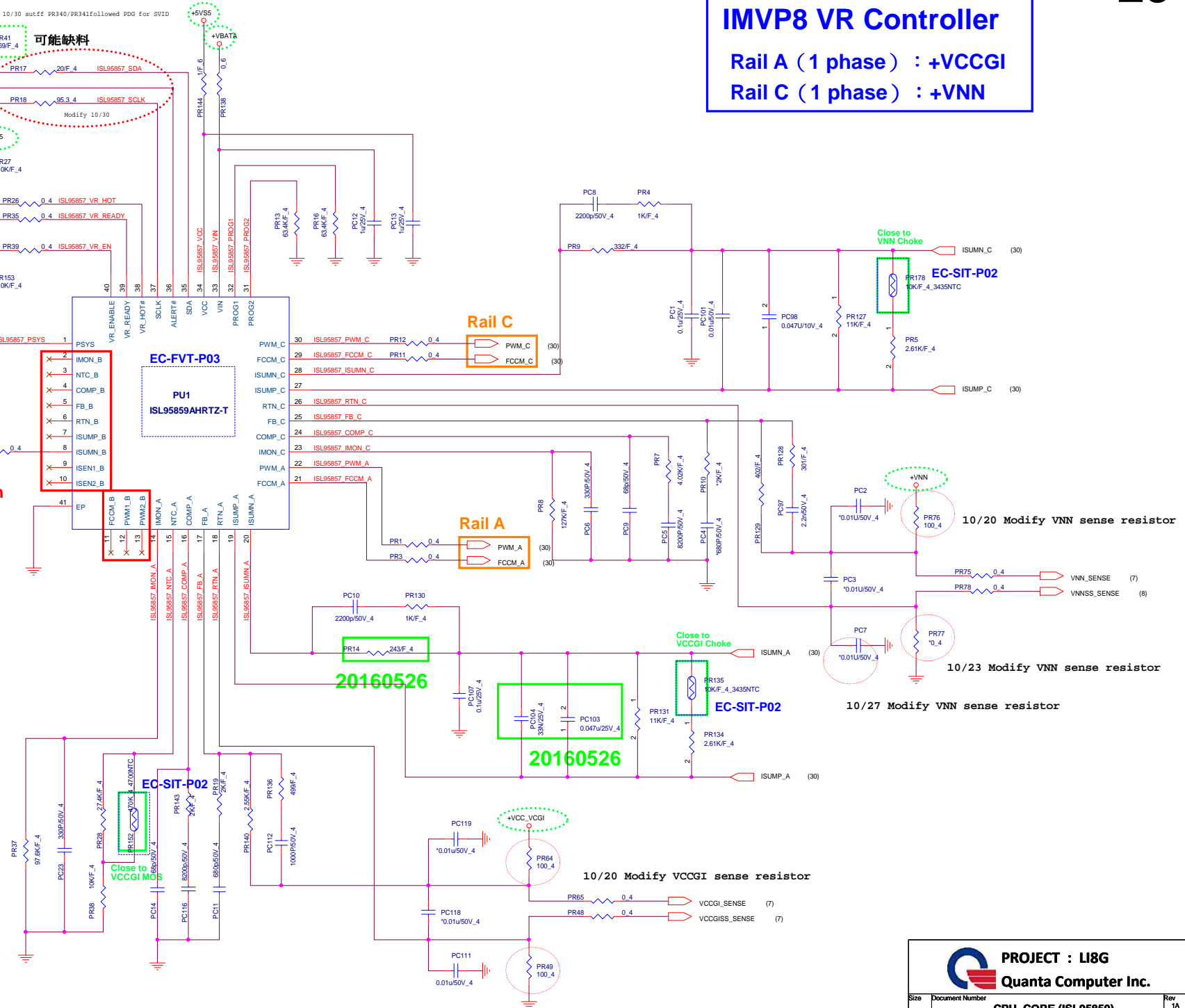
+VNN

Icc Max : 4.8A
 Icc TDC : N/A
 Vboot : 1.05V
 OCP : 8A
 Fsw : 750KHZ

VCCGI L/L :

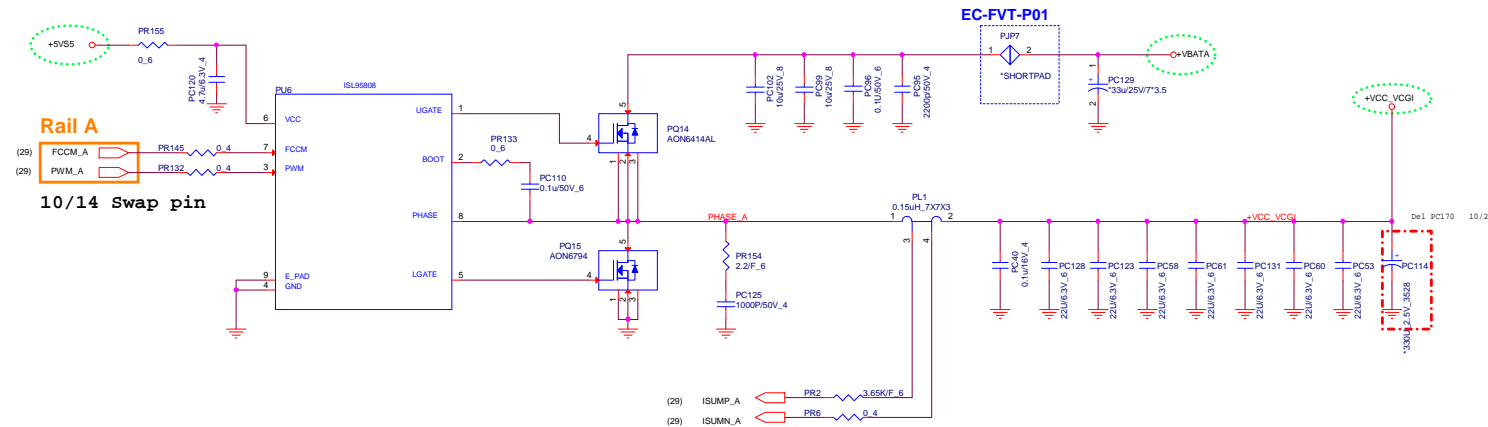
R_DC_LL : 6mV/A
 R_AC_LL : 6mV/A

Vinafix.com



(13,26,27,28,29,34,35)	+VBATA	
(7,29)	+VCC_VCGI	
(7,29)	+VNN	
(13,20,24,27,28,29,33,35)	+5VS5	

VCCGI



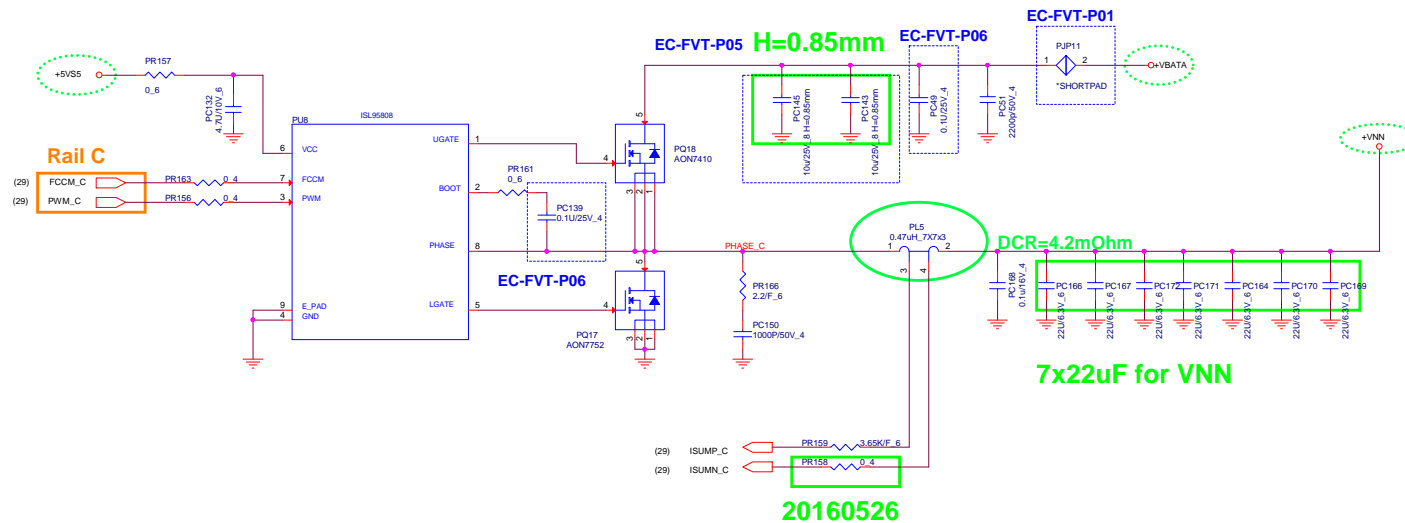
+VCCGI

Icc Max : 21A
Icc TDC : 18A
Vboot : 0V
OCP : 25A
Fsw : 750KHZ

VCCGI L/L :

R_DC_LL : 6mV/A
R_AC_LL : 6mV/A

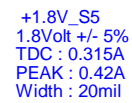
VNN



+VNN

Icc Max : 4.8A
Icc TDC : N/A
Vboot : 1.05V
OCP : 8A
Fsw : 750KHZ

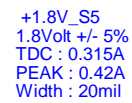
+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil



+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil

+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil

+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil



+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil

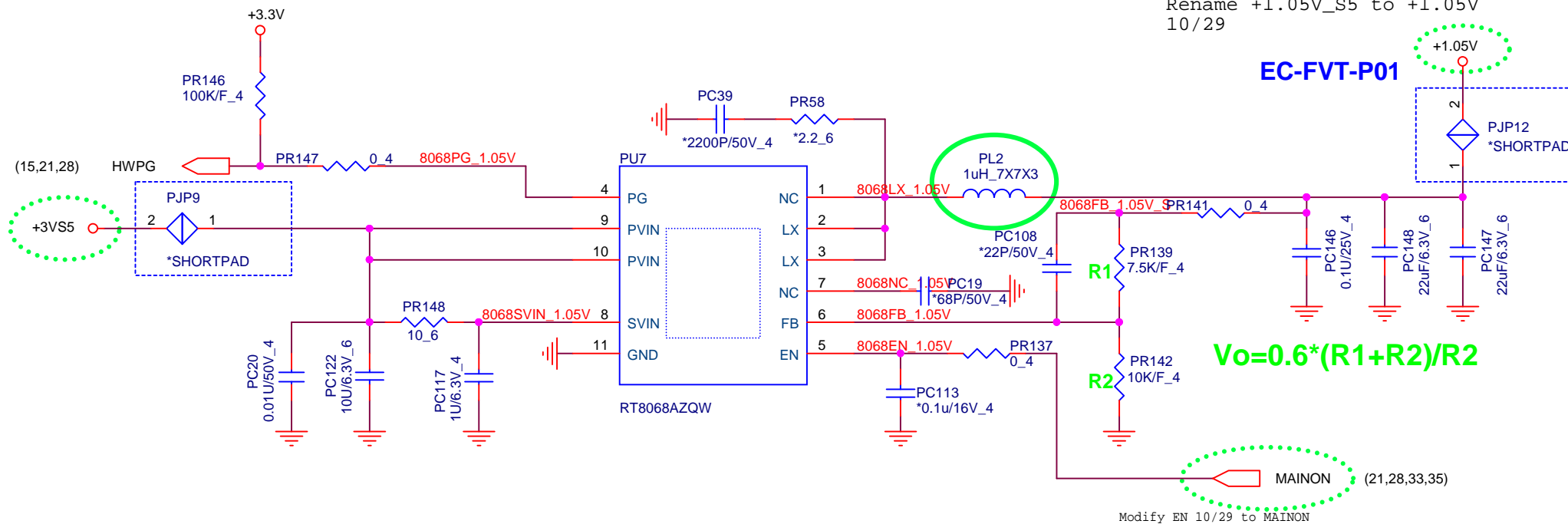
+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil

+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil

+1.05V_S5
1.05Volt +/- 5%
TDC : 2.025A
PEAK : 2.7A
Width : 100mil

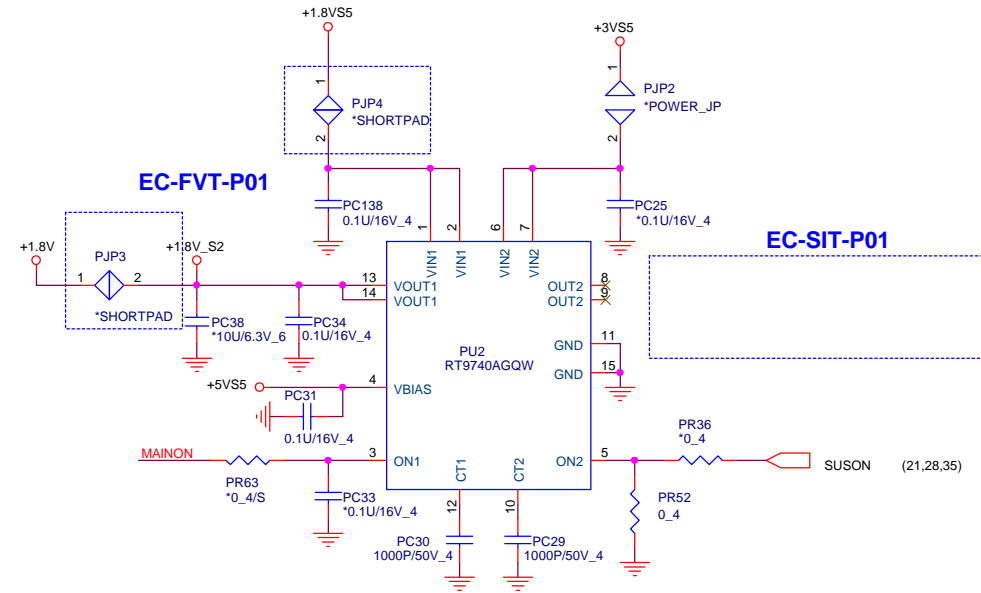
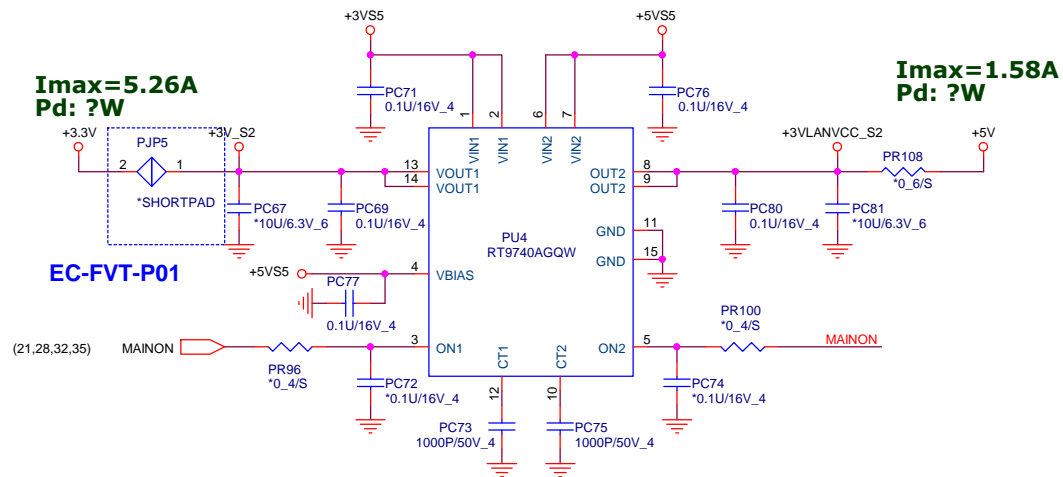
Rename +1.05V_S5 to +1.05V
10/29

EC-FVT-P01



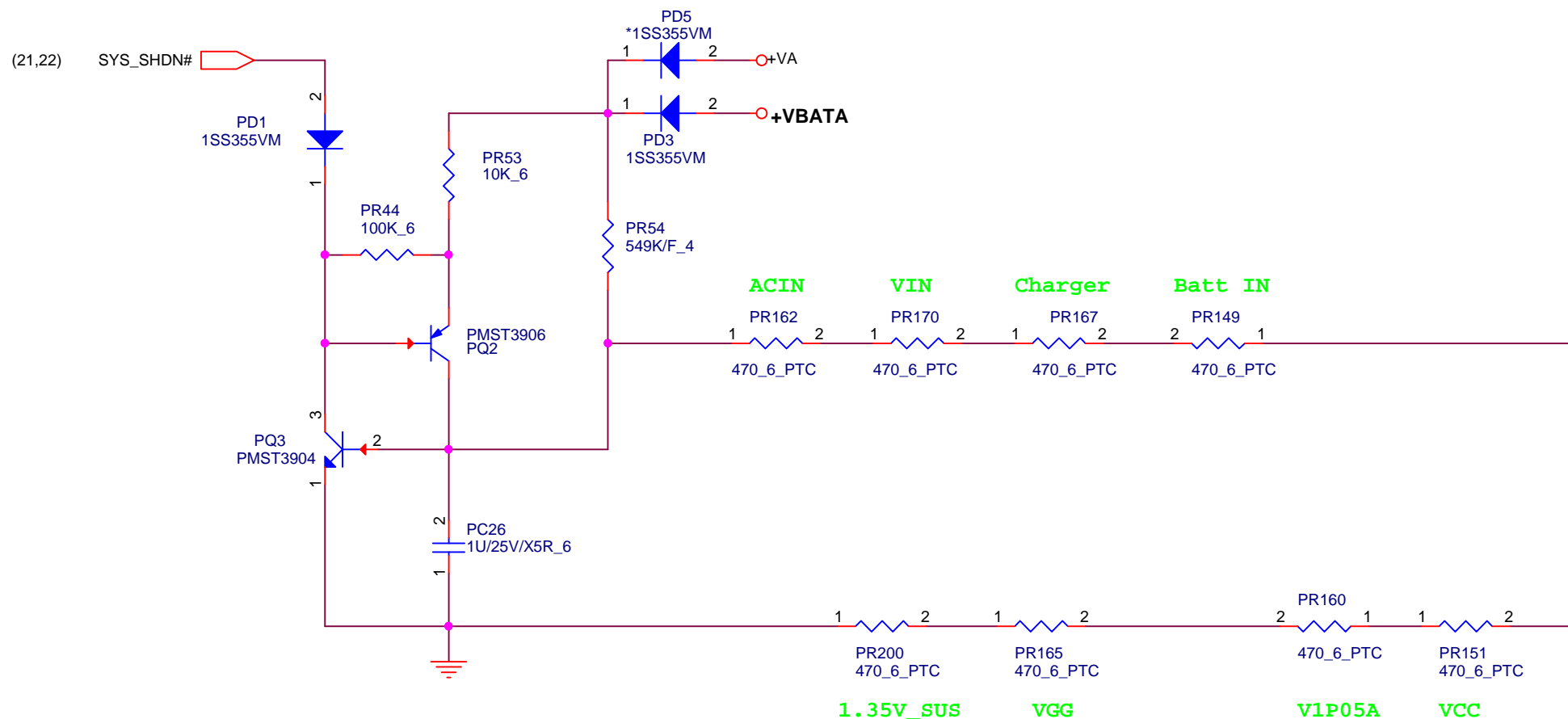
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V (RT8068AZQW)	1A
Date:	Thursday, September 08, 2016	Sheet 32 of 40



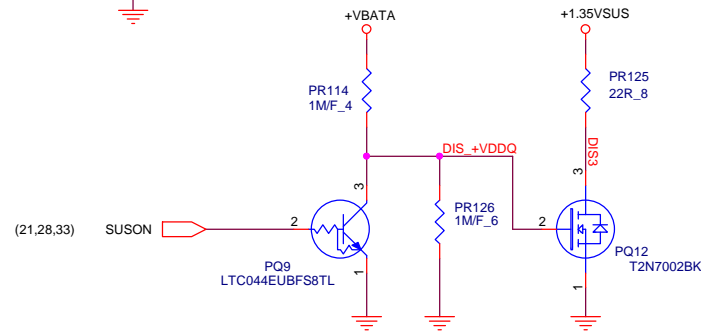
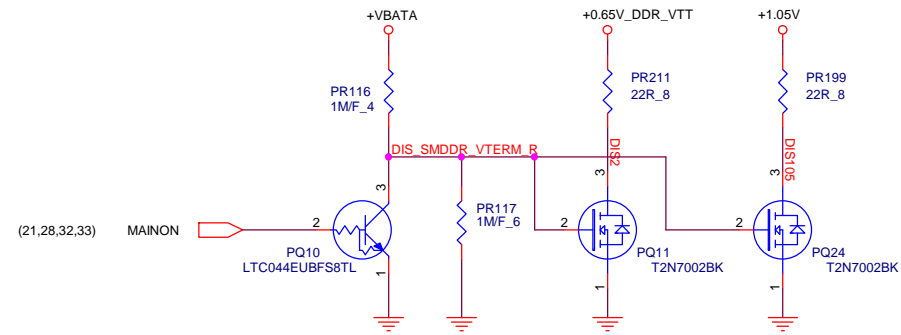
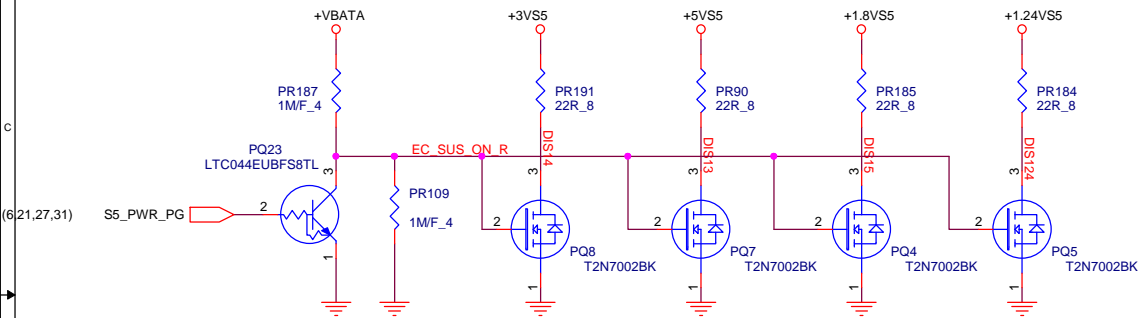
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	Load SW	1A
Date:	Thursday, September 08, 2016	Sheet 33 of 40



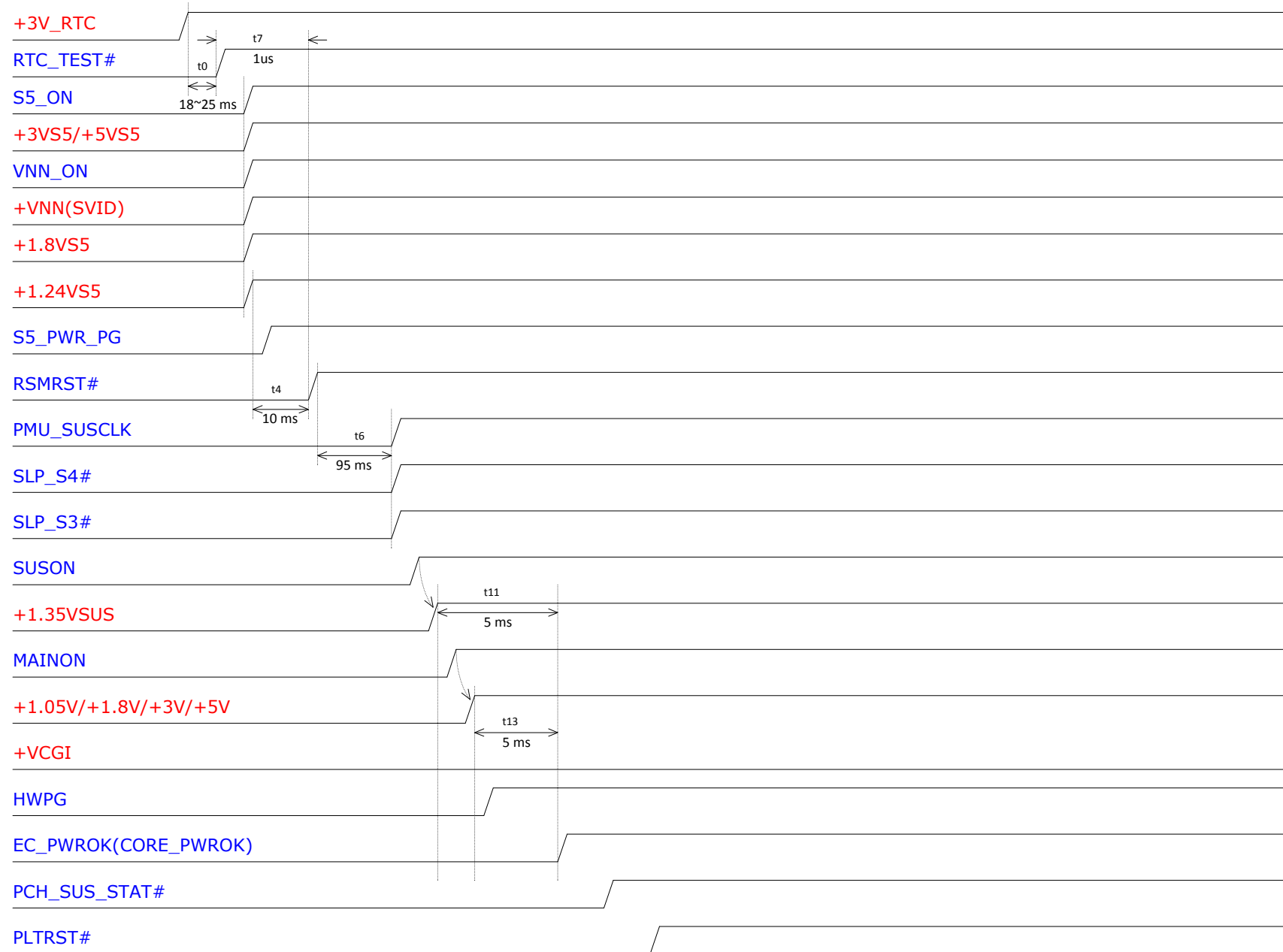
DISCHARGE

35



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	1A
Date:	Thursday, September 08, 2016	Sheet 35 of 40



PROJECT : LI8G
Quanta Computer Inc.

Size Document Number
Date: Thursday, September 08, 2016 Sheet 36 of 40

Power sequence

Rev. 1A

LI8 EE Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-FVT-01	24	Modify LED limited circuit resistor value the same as Newton 1.	R301,R306
EC-FVT-02	13	Buyer request change CAP PN due to EOD issue.	C238
EC-FVT-03	12	Stuff 100K to keep RSMRST# low after S5_ON ramped.	R321
EC-FVT-04	15	Add level shift for TPM reset pin.	Add Q47,R512,R507 Reserve Q46,R245
EC-FVT-05	21	S5_ON PU RES change to 10K to solve can't power on issue.	R468
EC-FVT-06	21	Modify R26/R21 PU power rail to solve can't power on issue.	
EC-FVT-07	12	Add CLKREQ# level shift circuit	Add U34,R510,R511 Reserve R508,R509
EC-FVT-08	3	Modify CLKREQ# PU power rail to +1.8VS5	
EC-FVT-09	15	Modify TPM footprint for pin4/pin11	U14
EC-FVT-10	18	RDC request to modify SSD CONN footprint	CN16
EC-FVT-11	3	Un-stuff BIOS ROM socket	Delete U29,U16 Add U17
EC-FVT-12	10	Un-stuff XDP CONN	Delete CN4
EC-FVT-13	5	Modify BID for FVT stage	Un-stuff R325; Stuff R342
EC-FVT-14	16,24,14	Follow ESD team request to modify ESD component P/N	SC8,SC13 Add EC8
EC-FVT-15	21	Un-stuff ESD component	Delete SC20
EC-FVT-16	6	Intel recomand to un-stuff RSMRST# & CORE_PWROK PU RES	Delete R391,R396
EC-FVT-17	21	Change RES value	R436
EC-FVT-18	5,16	Delete components which is workaround for ES sample CPU	Delete R145,R140,R146
EC-FVT-19	21	Modify EC pin11 VCC power rail to fix 3VPCU can't drop to 0V while press reset button	Add R13 Delete R19

D

LI8G EE Schematic EC Tracking Record B to C version(FVT -> SIT Planar)

EC #	Page	Description	Part Affected
EC-SIT-01	5	Modify KB LED GPIO to fix LED always on issue	
EC-SIT-02	21	Add MOS to turn off S5_ON while press EC reset button	Add Q50,R517
EC-SIT-03	16	Un-stuff Q30 to fix external MIC no function issue	Delete Q30 ; Add R484
EC-SIT-04	22	Modify MOS enable pin to fix press 4s power button shut down can't power on issue	
EC-SIT-05	22	Un-stuff diode and replace it with 0ohm	Delete D19 ; Add R513
EC-SIT-06	22	Modify PU RES value to 10K	R479
EC-SIT-07	22	Modify PTC circuit RES value to 100K	R458
EC-SIT-08	24	Un-stuff power on LED due to light leakage issue	Delete LED2,R284
EC-SIT-09	3	Follow Intel DG to PD USB2_VBUS_SNS	Delete R106 ; Add R113
EC-SIT-10	3	Follow Intel DG to PD USB2_DUALROLE_ID oin and reserve PU RES	Delete R105
EC-SIT-11	24	Modify KB LED limited-current RES value to meet test criteria	R290,R294
EC-SIT-12	21,26	Connect battery enable pin to EC	Delete PR111 ; Add R515
EC-SIT-13	19	WLAN power connect to +3.3V directly	Delete F4 ; Add F10
EC-SIT-14	13,19	Delete diode & PU RES due to no leakage concern	Delete D9,D10,R171,R173 ; Add R518,R519
EC-SIT-15	16	Modify ACZ_BCLK_AUDIO CAP value to fix Jitter over Spec issue	C148
EC-SIT-16	6	Add diode to fix can't power on until plug RTC issue	Add D25
EC-SIT-17	6	Stuff RTC_RST circuit	Add R477,R478
EC-SIT-18	21	Modify power rail to fix S5 leakage issue	Delete R13 ; Add R19
EC-SIT-19	5	Reserve IERR function	Delete R328 ; Add Q27
EC-SIT-20	13	Delete MOS which is no used for LCD_BK_OFF function	Delete Q6
EC-SIT-21	6	Modify TP to larger one	TP17,TP21
EC-SIT-22	16	Modify RES value to fix BIOS beep no sound issue	R250
EC-SIT-23	21	Connect THRMTRIP# to EC GPIO pin directly(reserve)	
EC-SIT-24	21	Reserve test point	Add TP56,TP57,TP58
EC-SIT-25	5	Modify board ID for SIT stage	Delete R324,R342 ; Add R341,R325
EC-SIT-26	20	Change USB power switch PN to 1.5A	U27,U28
EC-SIT-27	13	PN EOD issue	C238
EC-SIT-28	24	Modify PN	R301
EC-SIT-29	20	PN EOD issue	R184

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

